7. SUBJECT DETAILS

7.6 IC APPLICATIONS

7.6.1 Objective and Relevance

7.6.2 Scope

7.6.3 Prerequisites

7.6.4 Syllabus

i. JNTU

ii. GATE

iii. IES

7.6.5 Suggested Books

7.6.6 Websites

7.6.7 Experts' Details

7.6.8 Journals

7.6.9 Findings and Developments

7.6.10 Session Plan

i. Theory

ii. Tutorial

7.6.11 Students' Seminar Topics

7.6.12 Question Bank

i. JNTU

ii. GATE

iii. IES

7.6.1 OBJECTIVE AND RELEVANCE

The main objective of this course is to make the students understand the importance of Linear and Digital ICs. This course is organized in to three parts. In the first part, this course presents the widely used OP-amp IC 741 and other Linear ICs like 555 timer, 565 PLL , filters as well as DAC and ADCs. It gives better understanding of operations for the various applications and limitations of different ICs and their remedies. In the second part, it deals with data converters. Third part, it deals with different digital circuits implemented using combinational and sequential logic and about their ICs.

7.6.2 SCOPE

The integrated circuits field is a rising domain in industry. This subject enabled us to have a thorough understanding of various practical linear and digital integrated circuits which will serve as a building blocks of analog and digital circuit design. This subject will enhance the student knowledge in analog and digital design methodology and in various circuit applications.

7.6.3 PREREQUISITES

Requires a background knowledge of Boolean algebra, number system, switching theory and logic design, network analysis, transistor design and analysis.

7.6.3.1 JNTU SYLLABUS

PART-I LINEAR INTEGRATED CIRCUITS

UNIT-I
OBJECTIVE
Upon completion of this unit students will know the design aspects, basic structure of an Operational amplifier. Also about it's characteristics, specifications and it's basic applications.

SYLLABUS
Integrated Circuits: Classification, chip size and circuit complexity, ideal and practical Op-amp, Op-amp characteristics, DC and AC characteristics, 741 Op-amp and its features, modes of operation-inverting, non-inverting, differential.

UNIT-II
OBJECTIVE
In this unit students will know how an Op-amp could be devised for different applications and what is their operation. Basic concepts of voltage regulators is also studied.

SYLLABUS
OP-AMP Applications: Basic application of Op-amp, instrumentation amplifier, ac amplifier, V to I and I to V converters, sample and hold circuits, Differentiators and Integrators, Comparators, Schmitt trigger, Multivibrators, introduction to voltage regulators, features of 723 Regulator.

UNIT-III
OBJECTIVE

Upon completion of this unit students will know the design aspects of active RC filters as well as about the various Oscillators and waveform generators.

SYLLABUS

Active Filters & Oscillators: Introduction, First Order and Second Order Low Pass, High Pass and Band Pass filters, Active Band Reject and All pass Filters. Principle of Operation and types of Oscillators -RC, Wien Bridge and Quardrature type. Waveform Generators- Triangular, Saw Tooth, Square wave

UNIT-IV

OBJECTIVE

At the end of this unit students will know the internal structure of 555 timer and how it is used as multivibrator and their applications also about the function and components of PLL and its applications.

SYLLABUS

Timers & Phase Locked Loops: Introduction to 555Timer, Functional Diagram, Monostable and Astable operations and Applications, Schmitt Trigger, PLL - Introduction, Block Schematic, Principles and Description of Individual Blocks of 565, VCO.

PART-II DATA CONVERTER INTEGRATED CIRCUITS

UNIT-V

OBJECTIVE

From this unit students will gain a knowledge on types of analog to digital and digital to analog converters circuits, their design, specifications and applications.

SYLLABUS

D-A and A-D Converters: Introduction, Basic DAC Techniques - Weighted Resistor type, R-2R Ladder Type, Different types of ADCs - Parallel Comparator Type, Counter Type, Successive Approximation Register Type and Dual Slope Type. DAC and ADC Specifications.

PART-III DIGITAL INTEGRATED CIRCUITS

UNIT-VI

OBJECTIVE

From this unit students will know the important logic families like TTL and CMOS, basic logic gates and implementations using these logic families, and about the family specifications and configurations.

SYLLABUS

Introduction: Classification of Integrated Circuits, Standard TTL NAND Gate - Analysis & Characteristics, TTL Open Collector Outputs, Tristate TTL, MOS & CMOS open drain and tristate outputs, Comparison of Various Logic Families, IC interfacing TTL Driving CMOS & CMOS driving TTL.

UNIT-VII

OBJECTIVE

Upon completion of this unit students will know about the design of various combinational logic circuits their design, ICs and applications.

SYLLABUS

Combinational Circuits ICs: Use of TTL-74XX series & CMOS 40XX series ICs, TTL Ics - Code converters, Decoders, Demultiplexers, Encoders, Priority Encoders, Multiplexers & Their Applications,

Priority Generators, Arithmetic Circuit ICs - Parallel Binary Adder/Subtractor using 2's Complement system, Magnitude Comparator Circuits.

UNIT-VIII
OBJECTIVE
In this unit students will know how to design various sequential logic circuits as per requirements, about their design, ICs and applications.

SYLLABUS
Sequential Circuits ICs: Commonly Available 74XX &CMOS 40XX series Ics - RS, JK, JK Master - Slave, D and T Type Flip-Flops & their Conversions, Synchronous and Asynchronous counters, Decade counters, Shift Registers & Applications.

7.6.3.2 GATE SYLLABUS

UNIT-I
Operational Amplifiers—Characteristics

UNIT-II
Op-amp applications

UNIT-III
Active filters and oscillators.

UNIT-IV
VCOs and timers

UNIT-V
Sample and hold circuits, A/D and D/A converters.

UNIT-VI
Logic families

UNIT-VII
Not applicable

UNIT-VIII
Not applicable

7.6.3.3 IES SYLLABUS

UNIT-1
Operational Amplifiers,

UNIT-II
Op-amp applications

UNIT-III
Active filters and oscillators
UNIT-IV
Not applicable

UNIT-V
Not applicable

UNIT-VI
Not applicable

UNIT-VII
Not applicable

UNIT-VIII
Not applicable

7.6.5 SUGGESTED BOOKS

TEXT BOOKS:

1. Linear Integrated Circuits - D Roy Chowdury, New Age International (P) Ltd, 3rd Ed., 2008.
2. Digital Fundamental - Floyd and Jain, Pearson Education, 8th Edition, 2005
3. Op-Amps and Linear Integrated Circuits - Concepts and Applictions by James M. Fiore, Cengage/ Jaico, 2/e, 2009

REFERENCES:

1. Modern Digital Electronics - RP Jain - 4/e - TMH, 2010
2. Op-Amps and Linear Ics - Ramakanth A. Gayakwad, PHI, 1987
3. Operational Amplifiers and Linear Integrated Circuits by K.Lal Kishore - Pearson, 2008
4. Operational Amplifiers with Linear Integrated Circuits, 4/e Wiliam D. Stanley, Pearson Education India, 2009

7.6.6 WEBSITES

1. www.deas.harvard.edu
2. www.manchester.ac.uk/research/areas
3. www.eecs.umich.edu/eecs/research/resprojects.html
4. www.kabuki.eecs.berkeley.edu/papers.html
5. www.bbd_bestoff.com/importers.
6. www.ece.uiuc.edu
7. www.pearsoned.co.uk

7.6.7 EXPERTS' DETAILS

INTERNATIONAL

1. Mr. UDAY KIRAN EDURI
University of Texas, Dallas.
email: uxe021000@utdallas.com

2. Mr. FRANCO MALOBERTI
University of Pavia, Pavia.
email: Franco.maloberti@utdallas.edu

3. Mr. P.J.HURST
University of California
email: phurst@ieee.org

4. Mr. D.M.HUMMELS
University of Maine.
email: hummels@eece.maine.edu

NATIONAL

1. Dr. S Mukhopadhyay
Professor, Electrical Engineering,
IIT, Kharagpur, pin: 721302
email : smukh @ ee.iitkgp.ernet.in

2. Dr. Alok Barua
Professor, Electrical Engineering,
IIT, Kharagpur, pin: 721302
email alok @ ee.iitkgp.ernet.in

3. Dr. S Sengupta
Associate Professor,
IIT, Kharagpur, pin: 721302
email: ssg @ ee.iitkgp.ernet.in

REGIONAL

1. Mr. L.Sangram Kishore
Vignan's Enggineering College, Guntur.

2. Mr. K.Giri Babu
Lakki Reddy Bal Reddy College of Engineering,
Vijayawada.

7.6.7 JOURNALS

INTERNATIONAL

1. IEEE Transactions on Instrumentation and Measurement.
2. IEEE Transactions on Microelectronics.
3. IEEE Transactions on Electronic Circuits.
4. IEEE Transactions on Industrial Electronics.
5. IEEE Transactions on Circuits and Systems

NATIONAL

1. IETE Journal of Education
2. Journal of Instrumentation and Control

7.6.8 FINDINGS AND DEVELOPMENTS

1. Nano Magnetic STT-Logic partitioning for optimum performance.- J Das, and S.M. Alam, IEEE Transactions on VLSI systems, January 2014,Vol-22, No.1.
2. A high performance reference circuit with optimized input offset Operational Amplifier using device mismatch model.- Kapil K. Rajput, Sanjay singh, Ravi saini Anil K.Saini, Journal of VLSI Design Tools & Technology, January- April-2013
3. On Chip Compensation of Ring VCO Oscillation Frequency changes due to Supply Noise and Process Variation. - Y.-S. Park and W.-Y.Choi., IEEE Transactions on Circuits and Systems. February 2012, Vol.59, No.2.

4. Power Scalable, Complex Bandpass/Low-Pass Filter with I/Q Imbalance Calibration for a Multimode GNSS Receiver. -Y. Xu, B. Chi, X. Yu, N. Qi, P.Chiang, and Z. Wang, IEEE Transactions on Circuits and Systems. January 2012, Vol.59, No.1.

5. A Two -Stage ADC Architecture with VCO - Based Second State. -A.K. Gupta, K. Nagaraj, and Y.R. Viswanathan. IEEE Transactions on Circuits and Systems. November 2011, Vol.58, No.11.

   Digital Compensation Techniques for Frequency - Translating Hybrid Analog -to- Digital converters. S.J. Mazlouman, S.Sheikhaei, and S.Mirabbasi, IEEE Transactions on Instrumentation and Measurement, Vol. 60, No.3, March, 2011

6. Analysis and Design Techniques for Supply -Noise Mitigation in phase-Locked loops, A.Arakali, S.Gondi, and P.K. Hanumolu, IEEE Transactions on Circuits and Systems, Vol.57, No.11, November 2010.

7. Coherent Spectral Analysis of ADC Using Filter Bank, C. Rebai, D. Dallet and P. Marchegay, IEEE Transactions On Instrumentation and Measurement, Vol. 53, June 2004

8. INL Reconstruction of A/D Converters via parametric spectral Estimation, Filippo Attivissima, Nicola Giaquinto, IEEE Transactions On Instrumentation and Measurement, Vol. 53, August 2004

9. A Reconfigurable High-frequency Phase-Locked Loop, F. R. Desousa and B. Huyart, IEEE Transactions On Instrumentation and Measurement, Vol. 53, August 2004

10. INL and DNL Estimation Based on Noise for ADC Test, M. D. G.. C. Flores, M. Negkeiros, A. A. Susin,

    IEEE Transactions On Instrumentation and Measurement, Vol. 53, October 2004

Sl. No	Topics in JNTU syllabus	Modules and sub modules	Lecture No.	Suggested Books	Remarks
UNIT-I					

1	Classification, Chip Size and Circuit Complexity	Objective and Relevance prerequisites and background classification of ICs IC chip size, 'Circuit Complexity.	L1	T1-Ch1, R2-Ch2	
2	Ideal and Practical Op-Amp	IC packages, Manufacturing designation for ICs Op-Amp Terminals	L2	T1-Ch1, R2-Ch2, R3- Ch1	GATE IES
		Ideal Op Amp characteristics equivalent circuits practical Op-Amp characteristics	L3		
3	Op-Amp characteristics DC and AC Characteristics	DC characteristics Offset voltages and currents, Thermal Drift	L4	T1-Ch3, R2-Ch5, R3-Ch1	GATE IES
		Frequency Response	L5	T1-Ch3, R2-Ch6	
		Frequency Compensation	L6	T1-Ch3, R2-Ch6	
		Slew Rate	L7	T1-Ch3, R2-Ch6	
4	741Op-Amp and its features	Block schematic of Op-Amp Difference amplifier Buffer, Level Translator Output stage	L8	T1-Ch2, R2-Ch2,3	GATE IES
		Pin configuration Schematic Circuit diagram of A741 and features	L9	T1-Ch2, R2-Ch2,3, R3- Ch1	
5	Modes of Operation Inverting Non-Inverting differential	Inverting Amplifier Non-inverting Amplifier, Differential amplifier Gain in all the modes	L10,11	T1-Ch2, R2-Ch3, R3-Ch1	GATE IES
UNIT-II					
6	Basic applications of Op-amp	Scale changer Inverter Summing amplifier Inverting and non-inverting summing amplifier	L12	T1 Ch-4,R2 Ch-7 R1 Ch-3,9	GATE IES
		Subtractor Adder- subtractor	L13	T1 Ch-4,R2 Ch-7 R1 Ch-3,9	

Sl. No	Topics in JNTU syllabus	Modules and sub modules	Lecture No.	Suggested Books	Remarks
8	Instrumentation amplifier	Circuit diagram Block diagram	L14	T1 Ch-4,R2 Ch-7 R3 Ch-2	GATE IES
9	AC amplifier V to I and I to V converters	Inverting and non-inverting AC amplifier AC voltage follower Voltage to current and current to voltage converters	L15	T1 Ch-4,R2 Ch-7, R3 Ch-2	GATE IES

10	Sample and hold circuits Multipliers and dividers	Sample and hold circuits Input and output waveforms Multiplier schematic symbol and operation Multiplier IC configured as divider	L16	T1 Ch-4,R2 Ch-9, R3 Ch-2	GATE IES
11	Differentiators and integrators	Op-amp as differentiator Op-amp as integrator	L17	T1 Ch-4,R2 Ch-7, R3 Ch-1	GATE IES
12	Comparators Schmitt trigger	Inverting and non-inverting comparators Circuit diagram of Schmitt trigger Input and output waveforms	L18	T1 Ch-5,R2 Ch-9, R3 Ch-2	GATE IES
13	Multivibrators	Astable multivibrator Monostable multivibrator	L19	T1 Ch-5,R1 Ch-9, R2 Ch-8, R3 Ch-2	GATE IES
14	Introduction to voltage regulators Features of 723	Classification of voltage regulators Block diagram Pin diagram Features	L20	T1 Ch-6,R2 Ch-10, R3 Ch-6	GATE IES
		UNIT III			
15	Introduction 1st, 2nd order LPF & HPF filters	RC-Active 1st , 2nd order LPF	L21	T1-Ch7, R2-Ch8, R3-Ch3	GATE IES
		RC-Active 1st, 2nd order HPF	L22	T1-Ch7, R2-Ch8, R3-Ch3	GATE IES
16	Band Pass filters	Narrow band pass filter, Wide band pass filters	L23	T1-Ch7, R2-Ch8, R3-Ch3	GATE IES
17	Active –Band Reject filter, All-Passfilter	Narrow band reject filter, Wideband reject filters All pass filters	L24	T1-Ch7, R2-Ch8, R3-Ch3	GATE IES
18	Principle of operation and types of oscillators RC, Wien Bridge and Quardrature type	Principle of operation and types of oscillators	L25	T1-Ch7, R2-Ch8	GATE IES
		RC, Wien Bridge and Quardrature type	L26	T1-Ch7, R2-Ch8	GATE IES
19	Waveform generators- triangular Sawtooth Square wave	Triangular wave generator circuit diagram Input and output waveforms Sawtooth waveform generator circuit diagram	L27	T1-Ch7, R2-Ch8	GATE IES
		Square waveform generator circuit diagram,	L28	T1-Ch7, R2-Ch8	GATE IES

Sl. No	Topics in JNTU syllabus	Modules and sub modules	Lecture No.	Suggested Books	Remarks
		UNIT-IV			
20	Introduction to 555 timer Functional diagram	Introduction to 555 timer Description of 555 timer functional diagram	L29	T1 Ch-8, R1 Ch9, R2 Ch-10,R3 Ch4	GATE

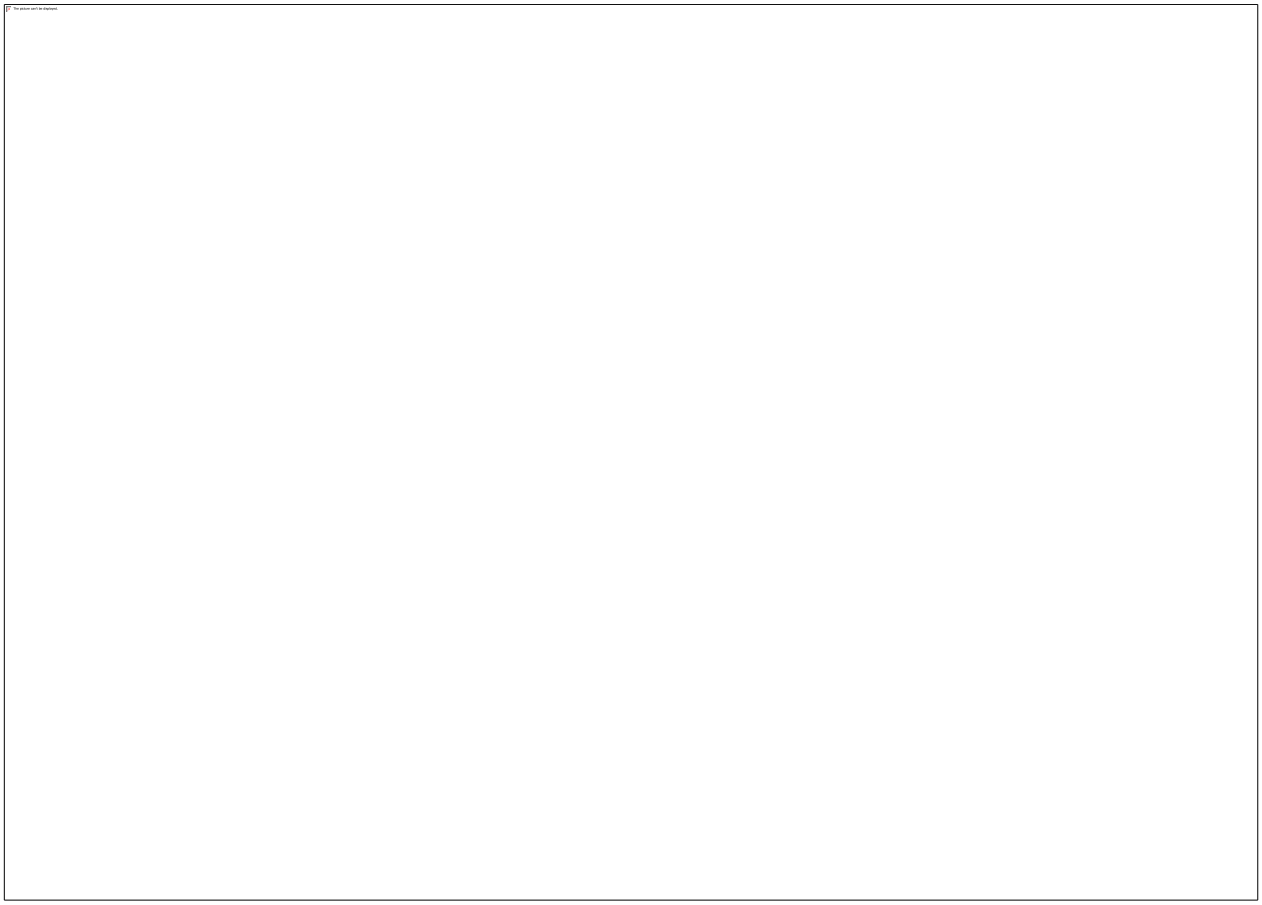
21	Monostable and astable operations and applications	555 timer as monostable multivibrator Applications of monostable Frequency divider Linear ramp generator	L30	T1 Ch-8, R1 Ch-9, R2 Ch-10, R3 Ch4	GATE
		555 timer as astable multivibrator Applications of astable Free running ramp generator	L31	T1 Ch-8, R1 Ch-9, R2 Ch-10, R3 Ch4	GATE
22	Schmitt trigger	555 timer as Schmitt trigger input and output waveforms	L32	T1 Ch-8, R1 Ch-9, R2 Ch-10, R3 Ch4	GATE
23	PLL-introduction Block schematic Principles and description of individual block of 565, VCO	Introduction to PLL Block schematic Basic principle	L33	T1 Ch-8, R2 Ch-10, R3 Ch4	GATE
		Description of individual blocks Phase detector Low pass filter	L34	T1 Ch-8, R2 Ch-10, R3 Ch4	GATE
		Error amplifier, VCO	L35		GATE
		UNIT-V			
24	Introduction Basic DAC techniques Weighted resistor DAC	Introduction Schematic of DAC Weighted resistor DAC using Op-amp	L36	T1 Ch-10,R1 Ch-10, R2 Ch-9, R3 Ch5	GATE
25	R-2R ladder DAC Inverted R-2R DAC	R-2R ladder DAC circuit diagram Inverted R-2R DAC circuit diagram	L37	T1 Ch-10,R1 Ch-10, R2 Ch-9, R3 Ch5	GATE
		IC 1408 DAC circuit diagram and pin configuration	L38	T1 Ch-10, R1 Ch10, R2 Ch-9 R3 Ch5	GATE
26	Different types of ADCs-parallel comparator type ADC	Functional diagram of ADC Types of ADCs Parallel comparator circuit diagram	L39	T1 Ch-10, R3 Ch5, R1 Ch-10,	GATE
27	Counter type ADC and successive approximation ADC	Counter type ADC Successive approximation ADC	L40	T1 Ch-10, R1 Ch10, R3 Ch5	GATE
28	Dual slope ADC DAC and ADC specifications	Functional diagram Output waveforms DAC specifications ADC specifications	L41	T1 Ch-10, R1 Ch10, R2 Ch-9, R3 Ch5	GATE

Sl. No	**Topics in JNTU syllabus**	**Modules and sub modules**	**Lecture No.**	**Suggested Books**	**Remarks**
		UNIT-VI			
29	Classification of integrated circuits Standard TTL NAND-gate-analysis characteristics	Classification of integrated circuits Standard TTL NAND gate circuit diagram Analysis Characteristics	L42	T2-Ch11, R1-Ch4	GATE
30	TTL open collector O/Ps Tristate TTL	TTL configurations Open collector Tristate TTL	L43	T2-Ch11, R1-Ch4	GATE

31	MOS and CMOS open drain and Tristate Output, CMOS transmission gate	MOS and CMOS Open drain MOS, CMOS Tristate and CMOS transmission gate	L44	T2-Ch11, R1-Ch4	GATE
32	Comparison of various logic families IC-interfacing-TTL driving CMOS and CMOS driving TTL	Comparison of various logic families IC interfacing TTL driving CMOS CMOS driving TTL	L45	T2-Ch11, R1-Ch4	GATE
		UNIT-VII			
33	Use of TTL-74XX and CMOS 40XX series	Introduction to TTL 74XX series Introduction to CMOS 40XX series	L46	T2-Ch6, R1-Ch4	
34	Code converters Decoders	Design of code converters Design of decoders	L47	T2-Ch6, R1-Ch6	
35	Demultiplexers	Demultiplexers Decoders and drives for LED display Decoders and drives for LCD display	L48	T2-Ch6, R1-Ch6	
36	Encoder, Priority encoder, Multiplexers and their applications	Encoder, Priority encoder, Multiplexers and their applications	L49,50	T2-Ch6, R1-Ch6	
37	Parity generators/ checker circuits	Parity generator Checker circuits	L51	T2-Ch6, R1-Ch6	
38	Arithmetic circuits-ICs, parallel binary adder/subtractor circuits using 2's complement system	Parallel binary adder circuits using 2's complement system Parallel binary subtractor circuits using 2's complement system	L52	T2-Ch6, R1-Ch6	
39	Magnitude comparator circuits	Magnitude comparator circuits	L53	T2-Ch6, R1-Ch6	
		UNIT-VIII			
40	Sequential Circuits Ics. Commonly available 74XX &CMOS 40XX series Ics	Introduction to Commonly available 74XX and CMOS 40XX series ICs	L54	T2-Ch7 R1-Ch4	

Sl. No	Topics in JNTU syllabus	Modules and sub modules	Lecture No.	Suggested Books	Remarks
40	RS, JK, JK Master Slave, D and T Type Flip-Flops	RS, JK, JK Master Slave, D and T Type Flip-Flops Truth tables, Excitation tables and ICs	L55, 56	T2-Ch7, R1-Ch7	
43	Flip Flop conversions	Convert one Flip-Flop in to another such as D to JK, T to JK etc.	L57	T2-Ch7, R1-Ch7	
44	Synchronous and Asynchronous counters	Synchronous and Asynchronous counters	L58	T2-Ch8, R1-Ch8	
45	Decade counters Shift registers and Applications	Decade counters Shift registers and Applications	L59	T2-Ch8,9, R1-Ch8	

ii. TUTORIAL



1. STUDENTS' SEMINAR TOPICS

1. Anew High speed low power ! bit Full adder- Angshuman chakraborty, Sambhunath Pradhan., Journal of VLSI Design Tools & Technology, January- April-2013
2. On Chip Compensation of Ring VCO Oscillation Frequency changes due to Supply Noise and Process Variation. - Y.-S. Park and W.-Y.Choi., IEEE Transactions on Circuits and Systems. February 2012, Vol.59, No.2
3. Blind Adaptive Estimation of Integral Nonlinear Errors in ADCs using Arbitrary Input Stimulus -A.J.Gines, E.J. Peralias, and A. Rueda, IEE Transaction on Instrumentation and Measurement, Vol.60, No.2, February 2011.

4. Implement of Linear phase FIR Filters for a Rational Sampling-Rate conversion Utilizing the Coefficient Symmetry, R.Bregovic, Y.J.Yu, T.Saramaki, and Y.C.Lim, IEEE Transactions on circuits and Systems, Vol.58, No.3, March 2011
5. A state of the art on ADC error compensation methods, IEEE transactions on Instrumentation and measurement, August 2005

6. A digital tachometer for high temperature telemetry utilizing thermally uprated commercial electronic component, IEEE transactions on Instrumentation and measurement, August 2005

7. A framework for the characterization and verification of embedded phase locked loops, IEEE transactions on Instrumentation and measurement, Dec. 2003

8. Coherent Sprectal Analysis of ADC Using Filter Bank, C. Rebai, D. Dallet and P. Marchegay, IEEE Transactions On Instrumentation and Measurement, Vol. 53, June 2004

9. INL Reconstruction of A/D Converters via parametric spectral Estimation, Filippo Attivissima, Nicola Giaquinto, IEEE Transactions On Instrumentation and Measurement, Vol. 53, August 2004

10. A Reconfigurable High-frequency Phase-Locked Loop, F. R. Desousa and B. Huyart, IEEE Transactions On Instrumentation and Measurement, Vol. 53, August 2004

11. INL and DNL Estimation Based on Noise for ADC Test, M. D. G.. C. Flores, M. Negkeiros, A. A. Susin, IEEE Transactions On Instrumentation and Measurement, Vol. 53, October 2004

7.6.12 QUESTION BANK

UNIT-I

1. a) List and compare ideal and practical characteristics of an Op-Amp.
   b) What are the differences between the inverting and non-inverting terminals of Op-Amp? What do you mean by the term virtual ground? **(Dec 13)**

2. i. List the reasons for differences in ideal and practical non-inverting Op-Amp Amplifier.
   ii. Derive expressions for input and output impedances of a practical non-inverting Op-Amp amplifier.
   iii. Discuss how a voltage follower is built using an OP-Amp. **(Dec 12)**

3. i. Calculate
   a. Maximum output offset voltage caused by the input offset voltage V_{ios}
   b. Maximum output offset voltage caused by the input bias current. For an inverting amplifier with R1=100k, & R_f=10k. Here 741 OP-Amp is used with V_{ios}=6mV I_B=500nA. **(Dec 11)**

4. i. Explain the role of negative feed back in operational amplifiers.
   ii. How does negative feedback affect, the performance of an inverting amplifiers?
   iii. What are the three operating temperature ranges of the IC? **(Dec 11)**

5. i. Explain the various techniques used to compensate for thermal drift in op-amps.

ii. Explain the effects of time on input-offset voltage and input offset current. **(Dec 11)**

6. i. What is a level translator circuit? Why it is used with the cascaded differential amplifier?

ii. What si a cascode amplifier? List the characteristics of the cascode amplifier. **(Dec 11)**

7. i. Explain how the input off set voltage compensated for Op-amp.
   ii. How fast can the output of an Op-amp change by 10V, if its slew rate is 1V/s?
   iii. Define thermal drift **(May 11)**

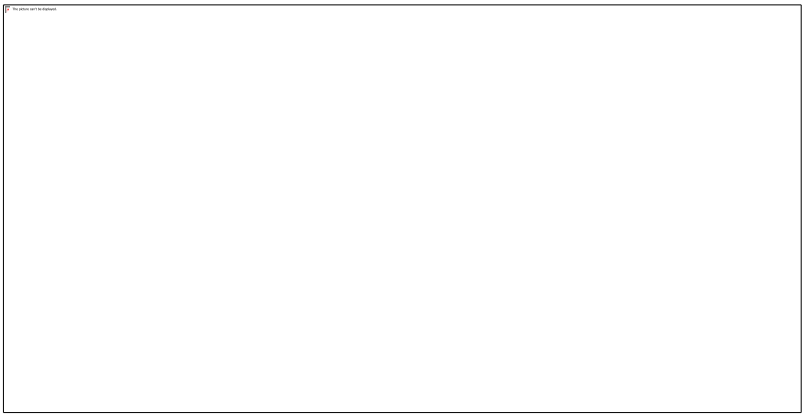
8. i. Explain the terms:
   a. CMRR.
   b. PSRR.
   c. Thermal drift.
   d. Inverting configuration of Op-Amp.
   ii. The 741IC Op-amp having the following amplifier with R1 = 1K , and RF = 10k, A=200000, Ri = 6 M, Ro = 150 , fo = 5 Hz, Supply voltages = 15 V, O/P Voltage Swing = 13V. Compute the values of
   a. AF closed loop voltage gain.
   b. fF bandwidth with feedback.
   c. Input resistance.
   d. Output Resistance. **(Nov 10)**

9. i. An op-amp has a slew rate of 2V/μs. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation. Derive the formulae used.
   ii. If the sinusoid of 10V peak is specified, what is the full power band width?
   iii. List out the non ideal Dc characteristics of an Op-amp? **(Nov 10, May 07)**

10. i. What are the three differential amplifier configurations? Compare and contrast these configurations.
    ii. What is a level translator circuit? Why is it used with the cascaded differential amplifier used in Op-amps?
    iii. Explain the term “Slew Rate" and how it affects the frequency response of an Op-amp? **(Nov 10)**

11. i. Draw the circuit diagram and explain the operation of an inverting amplifier, obtain the expression for closed loop voltage gain.
    ii. Derive the output voltage of an Op-amp based deferential amplifier. **(Nov 10)**

12. i. Give the design procedure of a compensating network for an Op-amp which uses $\pm$ 10V supply voltages. Assume necessary data.
    ii. In the circuit of Figure , R1 =100 , RF = 4.7K , CMRR=90 db. If the amplitude of the induced 60-Hz noise at the output is 5mV (rms). Calculate the amplitude of the common-mode input voltage V_{cm}. R_L=1k



(May 10)

13 i. Define input off set voltage and CMRR as applied to Op-amp ICs.
   ii. Explain how the above parameters can be measured? **(May 10)**

14. i. Broadly classify the integrated circuits for a wide range of applications.
    ii. What is a practical Op-amp? Draw its equivalent circuit.

iii. In an Op-amp, V2 = 0 (inverting terminal input). What is the voltage at V1 (non-inverting terminal input) for an output of 5V if A_{OL} = 50000. **(May 10)**

15. i. What is cross over distortions and how it is eliminated in differential amplifier? **(May 10, 08)**
    ii. Explain different methods of external frequency compensation in an Op-amp.
    iii. Design an amplifier with a gain of +5 using one Op-amp (make necessary assumptions).

16. i. Discuss DC characteristics of op-amp in detail.
    ii. What are the ideal characteristics of op-amp? **(Jan 10)**

17. i Discuss A.C characteristics of op-amp.
    ii. Compare closed loop and open lop configurations of op-amp. **(Jan 10)**

18. i. Compare Inverting, non-Inverting and differential configurations of op-amp. **(Jan 10)**
    ii. Draw and explain ideal and practical voltage transfer curves of op-amp.

19. i. Explain open loop configuration of op-amp. Draw its voltage transfer curve.
    ii. Draw the equivalent circuit of an op-amp and explain.
    iii. Compare open loop and closed loop configuration of op-amp. **(Jan 10)**

20. Explain in detail all the dc and ac characteristics of an ideal OP-AMP with relevant expressions. **(Jan 10, May 05)**

21. i. Derive closed loop voltage gain, input resistance, output resistance and bandwidth for inverting amplifier with feedback arrangement. **(May 08, 09, Jan 03)**
    ii. Explain any one of the frequency compensation technique in connection with Op-amp.

22. i. Derive the expression for CMRR for the first stage differential amplifier
    ii. Explain about any two linear and nonlinear applications of OP-AMP **(May 09, 06, 05)**

23. i. Define slew rate and derive the expression for it. List causes of the slew rate and explain its significance in applications.
    ii. Explain the difference between slew rate and transient response. **(May 09, 07, 03)**

24. i. With the help of a block diagram explain the basic building blocks of an op-amp.
    ii. What does the term 'balanced output' mean in an op-amp. **(May 09, Jan 03)**

25. i. List the parameters that should be considered for AC and DC application.
    ii. What are the three factors that affect the electrical parameters of an op-amp. (May 09, Jan 03)

26. i. Define the terms :SVRR, CMRR, input bias offset voltage, Gain Bandwidth product.
    ii. What are the differences between the inverting and non inverting terminals? What do you mean by the term "virtual ground"? (Aug, May 08, Sep 06, May 05)

27. i. Why is emitter resistor RE replaced by a constant current bias circuit in differential amplifier stage of an OP-AMP?
    ii. Explain why open loop configurations are not used in linear applications
    iii. For an OP-AMP, PSRR=70dB(min),CMRR=105,differential mode gain Ad=105. the output voltage changes by 20V in 4 microseconds. Calculate i) numerical value of PSRR (ii)Common mode gain iii) Slew rate of the OP-AMP. (Aug 08, May 06,05)

28. i. Give the pin diagram of IC741 and give its specifications. (May 08, 07)
    ii. Discuss the differences between the differential amplifiers used in the first two stagesof Op-amp.

29. Briefly explain why negative feedback is desirable in amplifier applications (May 08, 05, 04)

30. Discuss the electrical characteristics of an OP-AMP in detail (May 08, 04)

31. i. Draw an ideal voltage transfer curve of an OP-AMP
ii. what are the features of IC 741? (May 08, 04)

32. i. List and explain the two special cases of inverting amplifiers.
ii. What is a voltage follower? What are its features and applications?
iii. Derive the expression for the output voltage of a non inverting amplifier. (May 08, 04)

33. i. Why is it necessary to use an external offset voltage compensating network with practical op-amp circuits?
ii. Compare and contrast an ideal op-amp and practical op-amp. (May 08, 03)

34. i. Explain the precautions that can be taken to minimize the effect of noise on an OP-AMP circuit.
ii. Calculate the effect of variation in power supply voltages on the output offset voltage for an inverting amplifier circuit. (May 08, Dec 04)

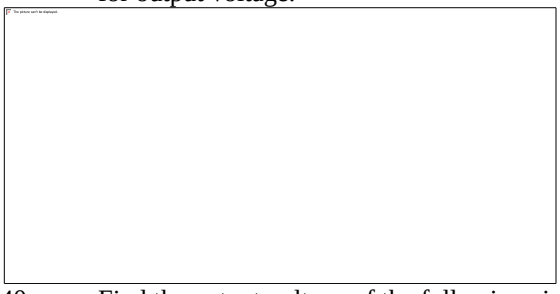
35. i. Explain the open loop and closed loop operations of an Op-amp.
ii. Explain different methods to increase the input resistance of an Op-amp. (Aug, May 07)

36. i. What are the three differential amplifier configurations? Compare and contrast these configurations.
ii. What is a level translator circuit? Why is it used with the cascaded differential amplifier used in Op-amps?
iii. Explain the term "Slew Rate" and how it affects the frequency response of an Op-amp? (Aug 07)

37. i. Draw a circuit using OP-AMP ,which can work as adder (inverting and non-inverting) and explain how it works.
ii. What is an OP-AMP? Why it is called so? (Sep 06, May 05)

38. What is a summer? Design a summer to add 4 input voltages in inverting configuration. (May 05, 04)

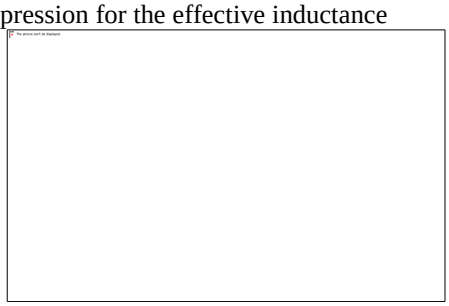
39. Draw the circuit diagram of a two input non inverting type summing amplifier and derive the expression for output voltage.



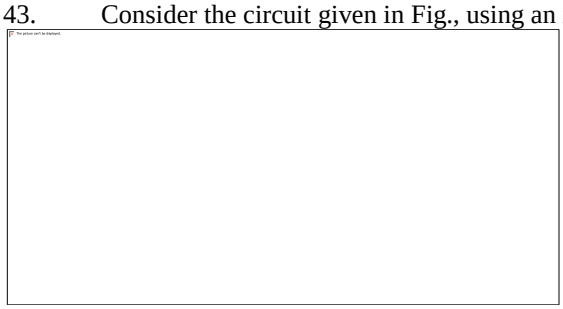
40. Find the output voltage of the following circuit, assuming ideal op-amp behavior. **(GATE 94)**

41. Sketch the output as a function of the input voltage (for negative values) for circuit shown in Fig. Show all the OP-AMP, and forward drop of the diode D_1=0. **(GATE 95)**

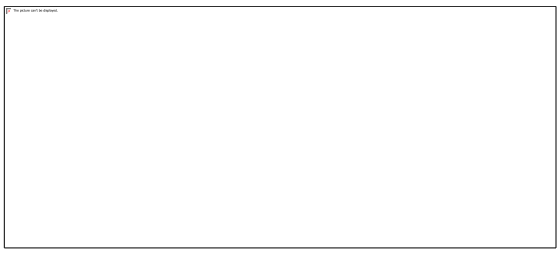
42. Assuming ideal op-amps, show that the circuit shown in Fig. simulates an inductor, i.e. show that $V_i(s)/I_{i(s)}$ is inductive and write the expression for the effective inductance **(GATE 96)**



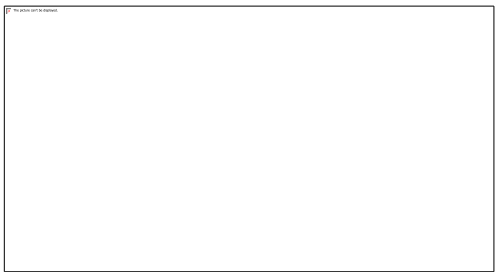
43. Consider the circuit given in Fig., using an ideal operational amplifier **(GATE 97)**



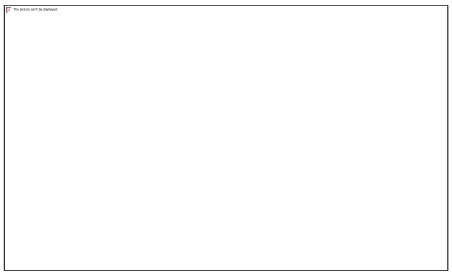
44. In the circuit shown in Fig., assume that the operational amplifier is ideal and that V_o=0V initially. The switch is connected first to 'A' charging C_1 to the voltage V. It is then connected to the point 'B'. This process is repeated f times per second **(GATE 97)**



45. Develop the voltage transfer function V_o/V_s for the amplifier shown **(GATE 95)**



46. Determine the input impedance of the circuit of Fig. And investigate if it can be inductive **(GATE 98)**

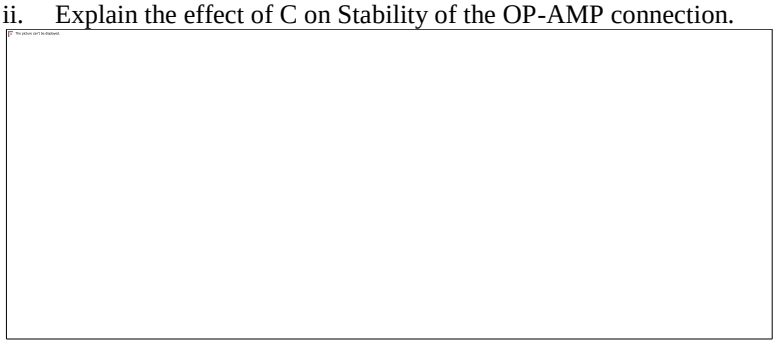


UNIT-II

1. a) Explain the working of an ideal active differentiator.
   b) Draw and explain the operation of an op-amp as an integrator. **(Nov 13)**

2 i. What is the operation performed by an inverting Op-Amp amplifier if its feedback resistance is replaced by a capacitance? Explain the functioning of such circuit. What are the practical difficulties associated with this circuit?
   ii. What is the purpose of an n-channel MOSFET in a typical OP-Amp based sample and Hold Circuit? Explain through circuit operation and relevant waveforms.
   iii. Explain the operation of an Op-Amp astable multivibrator used as square wave generator. Suggest a method to restrict its output swing to predetermined values. **(Nov 12)**

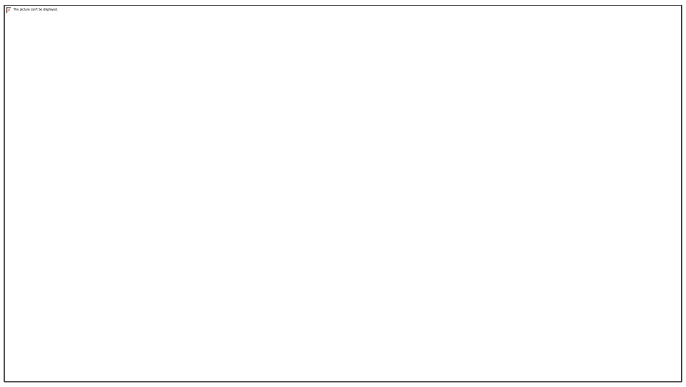
3. Consider the circuit shown in figure.
   i. Calculate the output voltages of the circuit.
   ii. Explain the effect of C on Stability of the OP-AMP connection.



(Dec 11)

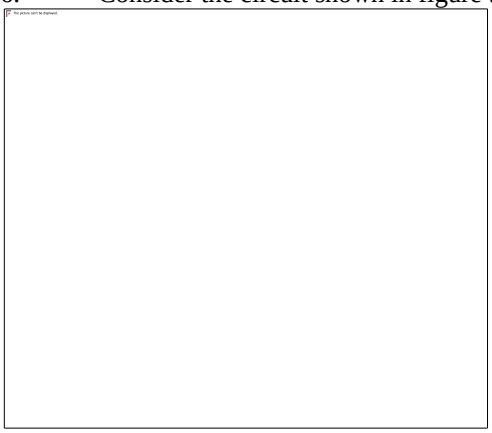
4. i. Explain how LF 398 can be used a sample and hold circuit?
   ii. Draw the wave forms of inverting and non-inverting comparator? **(Dec 11)**

5. i. Explain what the circuit does as shown in figure and explain its working



ii. What is the maximum value for Vin when the potentiometer is set to its maximum resistance? **(Dec 11)**

6. Consider the circuit shown in figure :



i. Ix
ii. V_A
iii. V_B
iv. Expression for V_A & V_B in terms of V1 & V2 **(Dec 11)**

7. Write short notes on:
i. Voltage - to - Frequency converter
ii. Monostable mulitvibrator applications. **(May 11)**

8. Sketch the circuit of a logarithmic amplifier using one Op-amp and explain its operation. State its application.
(Nov 10, May 09)

9. i. What is a clipper? With circuit diagram, explain the operation of positive and negative clippers.
ii. Describe the principle of operation of a precision half wave rectifier with wave forms. **(Nov 10, May 09)**

10. Design a differentiator using Op-amp to differentiate an input signal that varies in frequency from 1KHz to 10KHz.
(Nov 10, May 03)

11. i. Discuss the operation of a log amplifier and derive the expression for output voltage.
ii. Design a current to voltage converter using Op-amp and explain how it can be used to measure the output of a photocell. **(Nov 10)**

12. i. Classify the types of Op-amp based multipliers. How a multiplier can be used to
a. Double the incoming frequency.
b. Detect the phase angle of a signal.

ii. Design a subtractor in non inverting configuration. **(Nov 10)**

13. What do you mean by sampling? Explain the basic circuit for sample and hold circuit. **(May 10, 08, 05)**

14. i. What is Gyrator circuit? Explain its operation with a neat circuit diagram.
    ii. What is a sample and hold circuit? Why is it needed? With neat circuit diagram, describe the operation of an Op-amp based sample and hold circuit. **(May 10, 09)**

15. i. What is a voltage follower? What are its features and applications?
    ii. What do you mean by sampling?
    iii. Explain basic circuit for sample and hold circuit. **(May 10)**

16. i. Explain with a neat circuit diagram the working of voltage to current converter with floating load and grounded.
    ii. Design a circuit to convert a 4 mA to 20mA input current to 0V to 10V output voltage. The circuit is powered from $\pm$15V regulated supplies. (Assume necessary data) **(May 10)**

17. i. What is the name of the circuit that is used to detect the peak value of the non sinusoidal input waveforms. Draw it's circuit and explain it's operation.
    ii. Draw any one multivibrator circuit using Op-amp and explain its operation and derive relevant expression for its time period. **(May 10)**

18. i. Explain the frequency of operation of Astable multivibrator using op-amp and derive the expression for frequency of oscillation.
    ii. Discuss the features of IC 723. **(Jan 10)**

19. i. Explain Practical integrator with suitable mathematical expression.
    ii. Obtain the frequency response of Practical integrator. What are its applications?
    iii. Design a Practical integrator circuit with a d.c gain of 10, to integrate a square wave of 10KHz. **(Jan 10)**

20. i. Explain the operation and derive the expression for the overall gain of the op-amp instrumentation amplifier.
    ii. Discuss the characteristics, limitation and application of a Comparator **(Jan 10)**

21. i. With the help of Transfer characteristics input and output waveforms explain the operation of Inverting Schmitt trigger circuit.
    ii. Draw the circuit and explain the operation of sample and hold circuit. **(Jan 10)**

22. i. Explain the operation of a Practical Comparator with the help of a neat diagram.
    ii. Compare and Contrast Schmitt trigger and Comparator. **(Jan 10)**

23. Draw a circuit using Op-Amp, which can work as adder (inverting and non-inverting) and explain how it works. **(May 09, Aug 08)**

24. i. Explain the operation of Zero crossing detector. **(May 09, Aug 08)**
    ii. Briefly mention the disadvantages of using Zero crossing detector and how it is overcome in Schmitt Trigger?

25. i. Design a subtractor circuit whose output is equal to the difference between the two inputs. Use a basic differential Op-Amp configuration.
    ii. Name the circuit that is used to detect the peak value of the non sinusoidal waveforms. Draw its circuit and explain the operation. **(Aug 08)**

26. Explain how Op-amp used as a integrator and differentiator. **(Aug 08)**

27. i. Discuss the functioning of a practical integrator and derive the necessary expressions.
    ii. Design a practical integrator circuit to properly process input sinusoidal wave forms up to 1 KHz. The input amplitude is 10mV **(Aug 08, Apr 07)**

28. Draw the circuit and explain the working of
    i. voltage to current converter
    ii. current to voltage converter. **(Aug 08, May 08, 05)**

29. In some measurements it is necessary to sense current from a transducer and convert it into voltage. For a three Op-amp realization of a current input instrumentation amplifier, derive the expression for Vo. **(May 08, 07)**

30. i. Draw the circuit diagram of a two input non inverting type summing amplifier and derive the expression for output voltage.
    ii. Briefly explain why negative feedback is desirable in amplifier applications.
    iii. How does negative feedback affect the performance of an inverting amplifier? **(May 08, Aug 07)**

31. i. What is a switching regulator? Draw the block diagram of a typical switching regulator and explain its operation. **(May 08, 05, Sep 06)**
    ii. What are the four types of voltage regulators? Compare the performance of these regulators.

32. i. Discuss important characteristics of a comparator and the limitations of Op-Amp as comparators.
    ii. Explain the operation of Schmitt trigger circuit. **(Aug 07)**

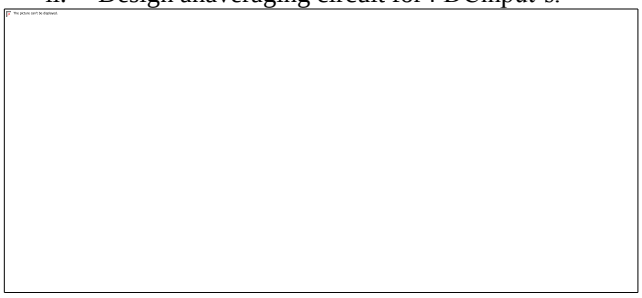
33. i. Explain with a neat circuit diagram the working of voltage to current converter with floating load and grounded.
    ii. Design a circuit to convert a 4 mA to 20mA input current to 0V to 10V output voltage. The circuit is powered from ±15V regulated supplies. (Assume necessary data) **(Aug 07)**

34. i. Explain HWR using inverting and non-inverting configuration.
    ii. Explain the operation of astable multivibrator using Op-amp. **(Aug 07)**

35. i. Explain the non-linear application of Op-amp as logarithmic and anti logarithmic amplifier.
    ii. Design a Integrator to integrate an I/P signal that varies in frequency from 1 KHz to 10 KHz and plot the O/P wave forms if the I/P is a sine wave of 1V peakat1KHz. **(May 07)**

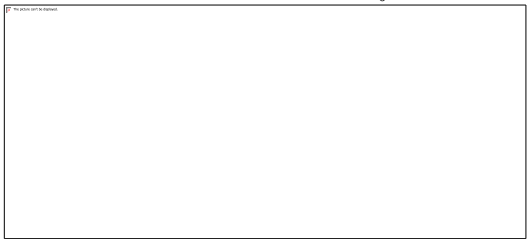
36. Design a practical integrator circuit to properly process input sinusoidal wave forms upto 1KHz. The input amplitude is 10mv. **(May 07, 03)**

37. i. In the circuit (figure) it can be shown in that $V_o = a_1V_1 + a_2V_2 + a_3V_3$.
    Find the values of a_1, a_2, a_3. Also find the value of V_o if
    i. R_4 is shorted circuited. ii. R_4 is removed. iii. R_1 is shorted circuited.
    ii. Design anaveraging circuit for4 DCinput's. **(May 07)**



38. i. What are the advantages of instrumentation amplifier? Derive an expression for the transfer function of an instrumentation amplifier. **(Sep 06, Nov 04)**
    ii. Explain the use of reference terminal provided in an integrated circuit instrumentation amplifiers.

39. Find the output voltage, V_0 in the following circuit, assuming that the op-amps are ideal **(GATE 93)**



40. Show that the system shown in Fig., is a double integrator. In other words, prove that the transfer gain is given by $[V_o(s)/V_s(s)] = [1/(CR_s)^2]$, assume ideal OP-AMP **(GATE 95)**

UNIT-III

1. a) Draw the circuit of RC phase-shift oscillator using op-amp. Derive expression for its frequency of oscillations?
   b) Design a wide band pass filter with f L=200Hz, f H=1kHz, and a pass band gain=4 using Op-Amps**.**
   (Nov 13)

2. i. List out the merits and demerits of active filters over passive filters.
   ii. Explain the functioning of any one RC type oscillator based on suitable circuit diagrams. What are the typical frequencies of oscillation? **(Nov 12)**

3. i Design a fourth order Butter worth low pass filter having upper cut o" frequency 1 KHz and pass band gain of 10.
   ii. Write about frequency transformation in active filter. **(Dec 11)**

4. i. With a neat diagram explain about triangular wave generator.
   ii. With a neat diagram, Explain about Saw tooth. Wave form generator. **(Dec 11)**

5. i. Define the conditions on the feed back circuit of an amplifier to convert it into an oscillator.
   ii. What is VCO? Give two applications of it.
   iii. Design a 60 Hz Active LPF. **(Dec 11)**

6. Design and Second Order IGMF band pass filter with the following specifications.
   f_O = 500 Hz, gain at resonance = -5 and band width = 50 Hz. Use the circuit shown in figure 4 assume necessary data
   (Dec 11)

7 i. Explain the frequency responses of all types of filters.
   ii. Figure shows the first order Butterworth of frequency. Give gain magnitude and phase angle equations
   (May 11)

8. i. Define the conditions on the feedback circuit of an amplifier to convert it in to an oscillator.
   ii. Design an RC phase shift oscillator for 300HZ frequency using ICμ A 741 and $\pm$15V power supplies. Assume necessary component values.

iii. Suggest a method to reduce the output voltage swing to I $\pm$6.5 Volts **(Nov 10)**

9. i. Define by means of a diagram the pass band, stop band, transition band and pass band ripple.
   ii. Sketch the ideal frequency-response characteristics of Low pass, high pass and band reject filters.
   iii. Design a second order low pass filter at a higher cut off frequency of 2KHz. **(Nov 10)**

10. i. Define Bessel, Butterworth and Chebyshev filters, and compare their frequency response.
    ii. Sketch the block diagram of I/II order band elimination filter and design a I order wide band- reject having f_H=200 Hz and f_L =1 kHz, having the pass band gain of 2 each. Assume necessary data. **(Nov 10)**

11. Design a wide band pass filter with f_L = 200Hz , f_H = 1 KHz and a pass band gain = 4.
    i. Draw the frequency response plot of this filter.
    ii. Calculate the value of Q for the filter. **(May 10, 08, 04)**

12. Write short notes on the operation of any two:
    i. Quadrature oscillator
    ii. RC phase shift oscillator
    iii. Wien- bridge oscillator **(May 10, Aug 07)**

13. i. classify the filters and explain the characteristics of each one of them.
    ii. Draw the first order low-pass Butterworth filter and analyze the same by deriving the gain and phase angle equation. **(May 10, 09)**

14. i. Explain the term “Frequency Scaling" with suitable example.
    ii. Design a I order wide band-pass filter with f_L=200 Hz. f_H=1 KHz and a pass band gain=4. Draw the frequency response and calculate ‘Q’ factor for the filter. (Assume necessary data) **(May 10)**

15. i. Design a II order Butterworth Low-pass filter for a cut off frequency of 1KHz and for a given normalized polynomial of S^2+1.414S+1. Assume necessary data.
    ii. In the above circuit given (figure) if the integrator components are
    R1=120 K and C1 = 0.01F, R3= 6.8 K R2= 1.2K, determine
    a. Peak-to-peak triangular output amplitude.
    b. The frequency of triangular wave. **(May 10)**

16. i. Compare RC phase shift and Wein bridge oscillators.
    ii. What are the advantages of active filters?
    ii. Discuss frequency response characteristics of various filters. **(Jan 10)**

17. i. What is an all pass filter? Explain its operation and applications areas.
    ii. Derive the expression for the magnitude of the transfer function and phase shift produced by the all pass filter. **(Jan 10)**

18. i. Explain the operation of 1st order low pass filter.
    ii. Design a First order low pass filter at a cut-off frequency of 400Hz and a pass band gain of 1. **(Jan 10)**

19. i. Explain the operation of RC-phase shift oscillator using op-amp and derive the expression for frequency of oscillations.
    ii. Design the RC phase-shift oscillator to have output frequency of 500Hz. Use 12V± supply. **(Jan 10)**

20. i. Derive the expression for frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit.
    ii. Design a second order low pass filter at a high cut off frequency of 1 KHz. Derive the transfer function of the above filter. **(May 09)**

21. Sketch the circuit of a logarithmic amplifier using one Op-amp and explain its operation. State its application.

(May 09)

22. i. Explain the operation of a delay equalizer circuit with neat sketches. Derive an expression relating input and output voltages of the equalizer.
    ii. For the all pass filter, determine the phase shift between input and output at f=2 KHz.
    iii. Give the condition for oscillations? **(Aug 08, May 07)**

23. .i. What are the advantages of active filters over passive once
    ii. Design a second order low pass butter worth filter for a cutoff frequency of 2 KHz assume necessary data

(Aug 08, May 05)

24. Design a Butterworth filter for a given normalized polynomial of S^2+ 1.4148S+ 1. Assume necessary data.

(May 08, Dec 04)

25. Design a notch filter for f_o =8kHz and quality factor Q=10. Choose C=500 pF and assume necessary data.

(May 08, 06, 05)

26. Explain the term "Frequency Scaling" with suitable example. **(May 08, Dec 04)**

27. i. Define a Notch filter. Give its application.
    ii. Determine the order of the Butterworth low-pass filter so that at w=1.5 w_{3dB}, the magnitude response is down by at least 30 dB.

(May 08, 04)

28. i. What are the advantages of active filters? Explain wideband band pass filter together with it?s amplitude response.
    ii. What is phase shifter? With respect to schematic explain the operation. **(May 08, Aug 07)**

29. i. Derive the transfer function for a general second order Sallen-key filter with suitable circuit diagram.
    ii. With suitable circuit diagram explain the operation of a triangular wave generator using a comparator and an integrator. **(May 08, Aug 07)**

30. i. The cutoff frequency of a certain first order low pass filter is 2KHz cover this low pass filter to have a cutoff frequency of 3KHz by using the frequency scaling technique.
    ii. What is the butter worth response? **(May 08, 03)**

31. i. Draw the circuit diagram of a low-pass Sallen key filter and determine it's gain.
    ii. Draw the block diagram of a band rejection filter and explain it's operation. **(Aug 07)**

32. i. Define the conditions on the feedback circuit of an amplifier to convert it in to an oscillator.
    ii. Design an RC phase shift oscillator for 300HZ frequency using IC µA 741 and ±15V power supplies. Assume necessary component values.
    Suggest a method to reduce the output voltage swing to I ± 6.5 Volts. **(May 07)**

33. i. Draw the schematic diagram of Wien Bridge Oscillator and derive the expression for frequency of oscillation.
    ii. What are the conditions to be satisfied by a circuit to produce oscillations? **(May 07)**

34. i. List the conditions for oscillation in all the three types of oscillators, namely, RC phase shift, wien- bridge and quadrature oscillators.
    ii. Explain the difference between a signal generator and a function generator.
    iii. Justify the name for quadrature oscillator. **(May 07)**

35. A certain narrow band pass filter has been designed to meet the following specifications: f_c = 2 khz, Q= 20 and Ap = 10. what modifications are necessary in the filter circuit to change the center frequency 'fc' to 1khz, keeping the gain and bandwidth constant? **(Sep 06, May 05)**

36. Explain the operation of a delay equalizer circuit with neat sketches. Derive an expression relating input and output voltages of the equalizer. **(Sep 06, May 04)**

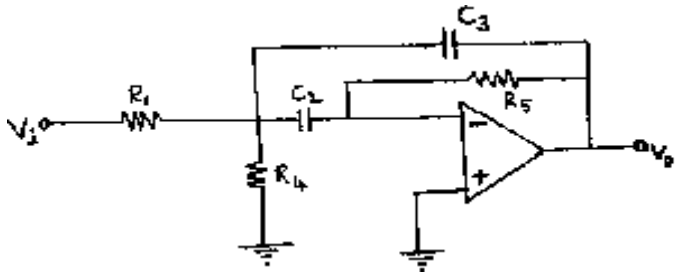
37. Design and obtain the frequency response of a band pass filter with f_L= 400Hz, f_H = 1KHz and the pass band gain =1. **(May 06, 05)**

38. i. Design the band pass filter with f_c = 1KHz, Q=3 and AF =10.
ii. Draw the frequency response and also change the center frequency to 1.5 KHz keeping AF and band-width constant. **(May 05)**

39. Draw the band pass filter circuit with its frequency response curve. Explain its working. **(May 05)**

40. i. Define Bessel, Butterworth and Chebyshev filters ,and compare their frequency response.
ii. Sketch the circuit diagram of band elimination filter and design a wide band reject having f_H=200Hz and f_L=1kHz. Assume necessary data. **(May 05)**

41. i. Derive an expression for the quality factor 'Q' of a twin- T notch filter. Give the suitable circuit diagram.
ii. Identify the given circuit and derive an expression for Bandwidth of the same circuit.

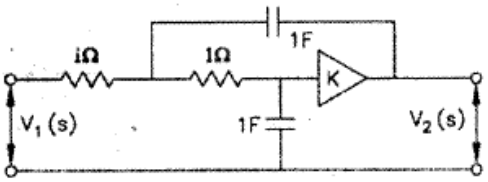


(Dec 04)

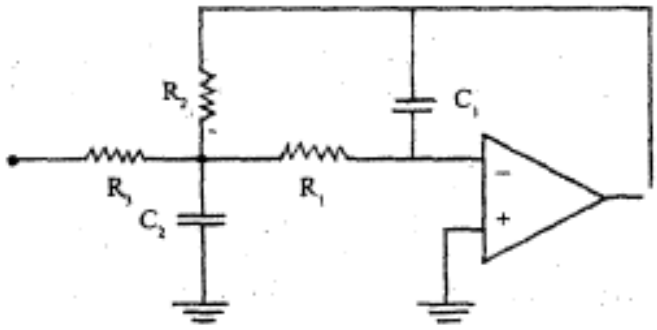
42. Design a first order high pass filter at a cutoff frequency of 400Hz and a pass band gain of 1. **(Nov 04)**

43. Assuming that the amplifier shown in the Fig. below, is a voltage-controlled voltage source, show that the voltage transfer function of the network is given by **(GATE 94)**

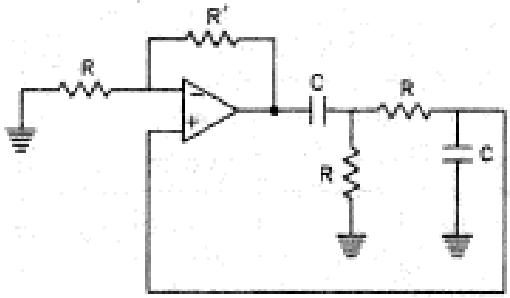
$$T = (s) = \frac{V_2(s)}{V_1(s)} = \frac{K}{2 + (3 - k)s + 1}$$



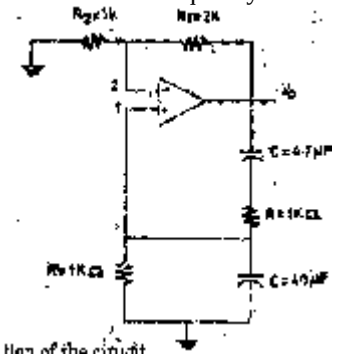
44. For the circuit shown find the damping factor and the cut-off frequency: **(IES 03)**



45. Find the value of R' in the circuit of Fig. For generating sinusoidal oscillations. Find the frequency of oscillations. **(GATE 98)**

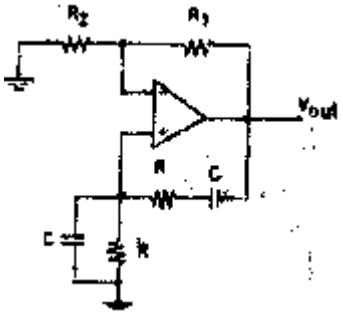


46. Determine the frequency of oscillation of the circuit shown in figure, assume op-amp is ideal.



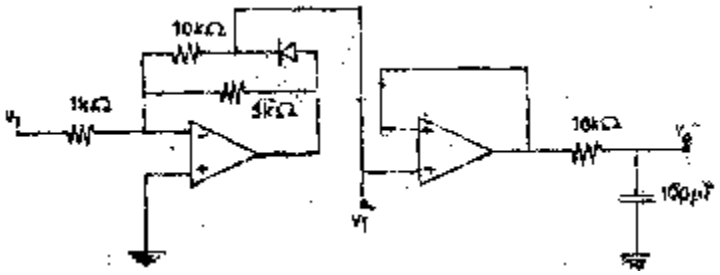
(GATE 00)

47. The circuit given in the figure will work as an oscillator at $f = 1/(2\delta RC)$, if R_1/R_2 is



(GATE 00)

48. The input voltage V_I in the circuit shown in the figure is a 1 KHz sine wave of 1V amplitude. Assume ideal operational Amplifier with ±15V DC supply
    i. Find the peak value of V_1
    ii. Find the average value of V_0 **(GATE 00)**



UNIT-IV

1. a) Explain the operation of 555 timer based Monostable multivibrator with functional diagram?
   b) Define
   i) Lock-in range
   ii) Capture range
   iii) Pull-in time. **(Nov 13)**

2. i. Discuss how a 555 timer can be used for FSK modulation, missing pulse detection, pulse width and pulse position modulation. State the mode of operation of 555 in each case.
   ii. What is the role played by a phase detector in the operation of a PLL? Explain through its block diagram. Define lock and capture ranges of a PLL. **(Nov 12)**
3. i. Describe the application of 555 timer as pulsing buzzer.
   ii. What are the functions of threshold and control voltage pins in 555 timer IC? **(Dec 11)**

4. i. How an symmetrical wave form generator can be constructed using 555 timer?
   ii. If RA = 6.8 k, RB = 3.3 k, c = 0.1 F in 555 astable multivibrator.
   Calculate:
   i. T_{high}
   ii. T_{low}
   iii. Free running frequency
   iv. Duty cycle. **(Dec 11)**

5. What is VCO? Give two applications of it. **(Dec 11)**

6. What are passive loop filters in PLL consider the PLL shown in figure?

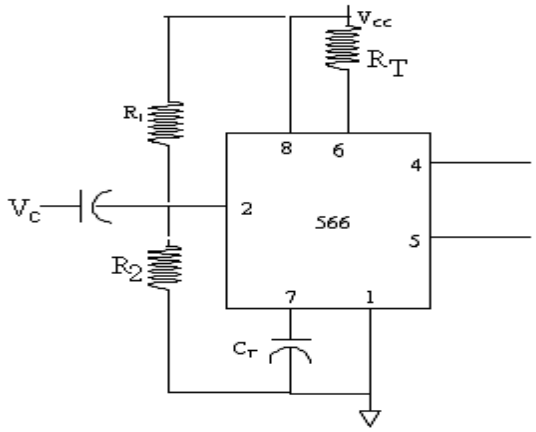
(Dec 11)

7. i. Write about voltage controlled frequency shifter using 555 timer.
   ii. For the frequency shifter calculate:
   i. The charge current I for input E = OV
   ii. The centre frequency when E = OV
   iii. The frequency shift fout for E = 1V. **(Dec 11)**

8. i. Design an astable multivibrator using 555 timer to produce a square wave of 2KHz frequency and 70% duty cycle. Draw the circuit with all component values.
   ii. Explain how a PLL is used as a frequency multiplier. **(May 11)**

9. i. Calculate the frequency of oscillation of a 566 VCO IC for the external component values RT = 6.8K and CT = 470PF. Assume other component values if necessary.
   ii. Draw the pin diagram of 566 VCO IC and list important specifications of 566VCO IC.**(Nov 10, May 06, 05)**

10. i. Calculate the frequency of oscillation of a 566 VCO IC for the external component values RT = 6.8K and CT = 470PF. Assume other component values if necessary shown in figure



   ii. Derive the expression for frequency of VCO and list important specifications of 566 VCO IC. **(Nov 10)**

11. i. Draw the schematic circuit diagram of the Analog phase detector.and explain their working. Derive necessary expressions.
   ii. What is their role is in PLL? Explain. **(Nov 10)**

12. i. Discuss any two applications of 555 timer in Monostable mode
   ii. Design a square waveform generatgor of frequency 1 kHz and duty cycle of 75% using 555 timer. **(Nov 10)**
13. i. Explain the role of the basic building blocks of PLL.
   ii. Determine the DC control voltage v_c at lock if signal frequency f_s = 10 KHz, VCO free running frequency is 10.66 KHz and the voltage to frequency transfer co-efficient of VCO is 6600 Hz / v. **(Nov 10, May 05)**

14. i. What is the phase-Locked loop? Briefly explain the roles of Low-pass filter and VCO in PLL.
   ii. Explain an application in which the 555 timer can be used as Astable multivibrator. **(May 10)**
15. i. Describe how frequency division and multiplication can be achieved using a Phase Locked Loop.
ii. Draw the circuit of a PLL AM detector and explain its operation. **(May 10)**

16. i. Write short notes on :
   a. Balanced Modulator.
   b. Voltage Controlled Oscillator.
   c. Digital Phase Detector.
   ii. Give any one applications of PLL and explain it in detail. **(May 10)**

17. i. Draw and explain astable multivibrator using IC 555. Draw the output and capacitor voltage waveforms.
    ii Describe the operation of PLL using its block diagram. **(Jan 10)**

18. i. Define Lock range, capture range and pull-in-time.
    ii. Derive the expression for Lock range of PLL.
    iii. Explain the transfer characteristics ofPLL. **(Jan 10)**

19. i. Draw and explain the functional block diagram of IC 555.
    ii. Discuss various applications of PLL. **(Jan 10)**

20. i. Describe the 555 time monostable multivibrator applications in
    a. pulse stretching b. Frequency c. Pulse Width Modulation **(May 09, 08, 06, 05)**
    ii. Describe Pulse Position Modulation (PPM) using 555 timer astable multivibrator.

21. i. List the application of IC 565PLL and briefly describe the role of the PLL in any of that application.
    ii. Referring to the circuit shown in figure 4b determine the free running output, lock range and the capture range.
    (May 09)

22. i. Give the block diagram of NE 565 PLL and explain the role of each block. Make circuit connections to track the incoming signal and explain its operations.
    ii. With neat sketches, explain the following terms:
    a. Lock-in-range b. Capture range c. Pull-in time.
    iii. Sketch the capture transient and explain why it is generated before locking? **(May 09, Dec 04)**

23. i. Briefly describe three uses of an analog multiplier. **(Aug 08)**
    ii. What do you mean by sampling? Explain the basic circuit for sample and hold circuit.

24. i. Design a 555 Astable multivibrator to operate at 10 KHz with 40% duty cycle.
    ii. Draw the circuit of PLL as frequency multiplier and explain its working. **(Aug 08, May 08, 07, 03)**
25. i. What is the phase-Locked loop? Briefly explain the roles of Low-pass filter and VCO in PLL.
    ii. Explain an application in which the 555 timer can be used as Astable multivibrator.**(Aug, May 08, May 07)**

26. i. Explain the operation of Monostable multivibrator using 555 timer. Derive the expression of time delay of a Monostable multivibrator using 555 timer. **(Aug 08, May 03)**
    ii. Design a Monostable multivibrator using 555 timer to produce a pulse width of 100m sec.

27. i. Explain the role of the basic building blocks of PLL.
    ii. Determine the DC control voltage V_c at lock if signal frequency f_s=10 KHz, VCO free running frequency is 10.66 KHz and the voltage to frequency transfer co-efficient of VCO is 6600 Hz/v. **(Aug 08, May 03)**

28. i. What is the role of the following blocks in the operations of PLL. Give the circuit diagrams and explain in detail
    a. Phase Comparator b. Low pass filter c. VCO.
    ii. Give any two applications of PLL. Explain in detail. **(Aug 08, Dec 04)**

29. i. Draw the circuit of Schmitt trigger using 555 timer and explain its operation. **(May 08, 05)**
    ii. How is an Astable multivibrator using 555 timer connected in to a pulse position modulator?

30. i. Derive the expression for frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit. **(May 08)**
    ii. Design a second order low pass filter at a high cut off frequency of 1 KHz. Derive the transfer function of the above filter.

31. How do we get a Notch filter from a band pass filter. **(May 08)**

32. Draw a circuit and explain in detail the two operating modes of the 555 timer with timing diagram. **(May 08, Jan 03)**

33. Give the functional block diagram of NE 565 PLL (DIP) and for the given component values. C_1 = 390PF, C_2 = 680PF and R_1 = 10k, Vcc = ±6V **(May 08, Sep 06, May 05)**
    i. Find the free running frequency
    ii. The lock range and capture range

34. i. Give the block diagram of PLL and explain about each block in detail.
    ii. Define the following terms with reference to PLL **(May 08, 04)**
    a. Lock range b. Capture range c. Pull-in-time

35. i. Draw the circuit of a PLL AM detector and explain its operation.
    ii. What is the major difference between digital and analog PLLs? **(May 08, 04)**

36. Describe any two applications of 555 timer in
    i. Astable multivibrator configuration.
    ii. Monostable multivibrator configuration **(Aug 07)**

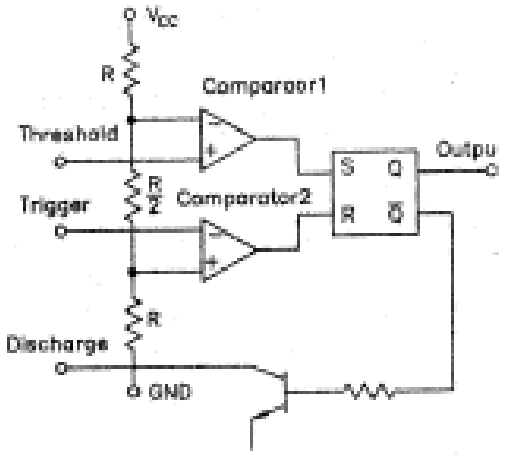
37. i. Give the functional block diagram of NE 565 PLL and for the given component values. C_1 = 390PF, C_2 = 680PF and R_1 = 10k,V_{cc} = ± 6V. Find
    a. The free running frequency.
    b. The lock range and capture range.
    Where C_1 is the capacitor connected between pin number 9 and - V_{CC}, C_2 is the capacitor connected between + V_{CC} and output pin 7, and R_1 is connected between pin number 8 and + V_{CC}.
    ii. Give the functional block diagram of VCO NE566 and explain its working and necessary expression for free running or center frequency **(Aug, May 07. Sep 06, May 05)**

38. i. Explain the operation of Astable multivibrator using 555 timer.
    ii. Design a Monostable multivibrator using 555 timer to produce a pulse width of 200 ms. **(Aug 07)**

39. i. Draw the block diagram of 565 PLL and explain about each block. Make circuit connections to track the input signal and explain its operation.
    ii. Write short notes on :
    a. PLL as frequency multiplier
    b. PLL as frequency translator **(Aug 07)**

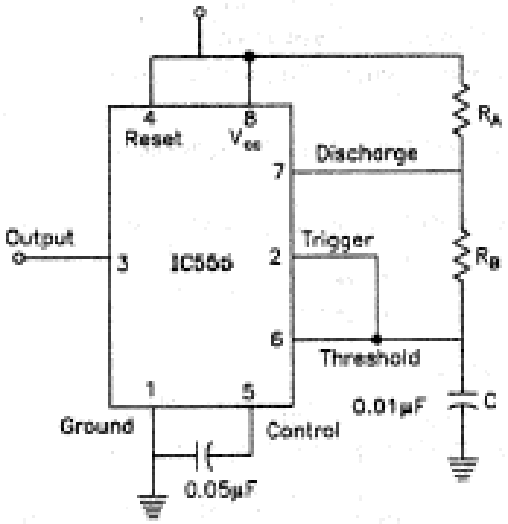
40. i. With necessary external components to a VCO IC NE556, Explain the generation of a triangular wave.
    ii. A PLL has a free running frequency of 500 KHz, the bandwidth of the LPF=1 KHz. Will the PLL lock in if f_i =60 KHz? What is the frequency of the VCO outputs? **(May 07)**

41. i. Explain the terms Lock range, Capture range and Pull-in time a PLL. How are Lock Range and Capture range determined? **(Sep 06, May 05)**
    ii. Design a PLL circuit using IC 565 to get
    a. Free-running frequency = 4.5 KHz
    b. Lock range of 2 KHz and
    c. Capture range = 100 Hz.
    Assume a supply voltage of + or - 10V. Show the circuit diagram with all component values.



42. Implement a mono-stable multivibrator using the timer circuit shown in Fig. Also determine an expression for ON time T of the output pulse **(GATE 98)**

43. An IC 555 chip has been used to construct a pulse-Generator. Typical pin connections with components is shown in Fig., For such as application. However it is desired to generate a square pulse of 10kHz.



45. Draw the internal block diagram of an IC PLL NE565 or equivalent. Explain how you will realize a frequency multiplier to multiply an input frequency by a factor of 12 by using this PLL **(GATE 00)**

UNIT-V

1. a) Explain the operation of weighted resistor DAC with neat circuit diagram
   b) List out different types of A/D converters. **(Nov 13)**

2. i. List the specifications and draw the pin configuration of IC 1408 DAC.
   ii. What is the significance of 'linearity' and 'conversion time' in an ADC?
   iii. Explain the operation of a weighted resistor type DAC. **(Nov 12)**

3. i. Explain the difference between Analog to Digital converter and Digital to Analog converters through underlying equations.
   iil. Illustrate one application each of Analog to Digital and Digital to Analog converters. **(Dec 11)**

4. i. Write a note on multiplying DACs.
   ii. Compare and contrast R-2R ladder type and weighted resistor type DACs.
   iii. List the specifications of a Digital-to-Analog converter IC, 1408. **(Dec 11)**

5. i. Explain the operation of parallel comparator type ADC with the help of a neat diagram.
   ii. The LSB of a 6-bit D/A converter represents 0.1V. What voltage value will be represented by the following binary words?
   i. 101010
   ii. 110110 **(Dec 11)**

6. i. Explain the operation of a Successive Approximation type analog to digital converter.
   ii. Calculate the number of bits required to represent a full scale voltage of 10V with a resolution of 5mV approximately. **(Dec 11)**

7. i. Determine the resolution of 16 bit D/A converter.
   ii. Explain flash conversion with a neat circuit for four bits. **(May 11)**

8. Write short note on:
   i. R-2R Ladder DAC
   ii. Inverted to R-2R Ladder **(Nov 10)**

9. i. Explain Functional diagram of successive approximation ADC
   ii. Explain counter type A/D converter **(Nov 10)**

10. i. The basic step of a 16-bit DAC is 10.3 mV. If 0000000011111111 represents 0V, what output is produced if the input is 1111111111011011?
    ii. Calculate the values of the LSB, MSB and full scale output for an 32bit DAC for the 0 to 20V. **(Nov 10, May 09)**

11. i. Explain the operation of a multiplying DAC and mention its applications.
    ii. A 12-bit D to A converter has a full-scale range of 15 volts. Its maximum differential linearity error is ± 1/2 LSB.
    a. What is the percentage resolution?
    b. What are the minimum and maximum possible values of the increment in its output voltage? **(May 10, Aug 07)**

12. i. Explain the operation of a counter type of Analog to Digital converter.
    ii. Specify the modifications necessary in the circuit for a time varying analog input voltage.
    iii. Calculate the conversion time for a full scale input incase of a 12-bit counter type Analog to Digital converter driven by 2MHz clock. **(May 10)**

13. i. List out various types of D/A converter and A/D converters and compare their merits and demerits.
    ii. Give the schematic circuit of successive approximations A/D converter and explain its operation **(May 10)**

14. i. List out various types of D/A converter and A/D converters and compare their merits and demerits.
    ii Give the schematic circuits of successive approximations A/D converter and explain its operations.

15. Write short notes on:
    i. Dual-slope A/D converter.
    ii. Charge balancing type Analog to Digital converter. **(May 10)**

16. i. Describe parallel comparator type ADC operation.
    ii. Compare Flash and dual slope ADCs. **(Jan 10)**

17. i. Explain Successive approximation ADC with the help of block diagram. Also illustrate conversion process.
    ii. An 8-bit successive approximation ADC is driven by a 1MHz clock. Find its conversion time. **(Jan 10)**

18. i. Draw the block diagram and explain the operation of dual slope A/D converter. What are its advantages and disadvantages?
    ii. Explain the performance parameters of ADC. **(Jan 10)**

19. i. Explain in detail the succession approximation type ADC?
    ii. Give the schematic circuit diagram of successive approximation type A/D converter & explain the operation of this system. **(May 09, 08, Nov 03)**

20. i. Differentiate between D-A and A- D CONVERTERS.
    ii. Explain D/A converter with R and 2R resistors. **(May 09)**

21. Explain different types A/D and D/A converters. **(May 09)**

22. i. Sketch the Analog output voltage for the given digital input code. **(Aug 08)**
    ii. What are the major disadvantages in this type?

23. i. Explain the operation of a dual slope type Analog to Digital converter.
    ii. A dual slope Analog to Digital converter uses a 16-bit counter and operates at 4 MHz clock rate. The maximum input voltage is +8volts. Find the value of integrator resistor 'R' if the maximum output voltage of the integrator is -6V after 2n counts for an integrator capacitor of 0.1μF. **(Aug 08, May 07, 05)**

24. i. Sketch and explain the transfer characteristic of a DAC with necessary equations.
    ii. LSB of a 9-bit DAC is represented by 19.6 m Volts. If an input of 9 zero bits is represented by 0 volts.
    a. Find the output of the DAC for an input, 10110 1101 and 01101 1011.
    b. What is the Full scale Reading (FSR) of this DAC? **(May 08, Aug 07, May 05)**

25. Explain the operation of the fastest analog to digital converter. What is the main draw back of this converter? Compare this converter with other types. **(Aug 08, May 05)**

26. i. List out different types of A/D converters.
    ii. Draw the schematic circuit diagram of dual-slope A/D converter and explain its operation. Derive expression for output voltage.
    iii. Compare dual-slope A/D converter with successive approximation A/D converter. **(May 08, 05, Sep 06)**

27. i. Draw the block diagram for a 2-bit parallel-comparator A/D converter and explain the operation of the
ii. Draw a schematic diagram of a ladder network D/A converter. Explain the operation of the converter.

28. i. Draw and compare the conversion times for tracking and successive approximation ADC devices.
    ii. A dual slope ADC uses a 12 bit counter and a 8 MHz clock rate. The max input voltage is +10V. The max integrator output voltage should be -8V, when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 micro farad. Find the value of the resistor of the integrator. **(May 08, May 03)**

29. i. Compare this A/D converter with parallel comparator type A/D converter.
    ii. Give the working principle of analog multiplexer. **(May 08, Nov 04)**

30. i. With an example explain the functional diagram of successive approximation ADC.
    ii. Draw the schematic circuit diagram of a Servo A/D converter and explain the operations of this system.
    iii. Compare Servo A/D with other types of A/D converters. **(Aug, May 07)**

31. Write short notes on:
    i. Counter type ADC devices.
    ii. Inverted R-2R Digital to Analog converter. **(Nov 10, May 07)**

32. i. Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage Vo.
    ii. Give the schematic circuit of an A/D converter widely used in digital volt-meters and explain its operation. Derive expression for output voltage. **(May 07)**

33. i. Draw the circuit of a Weighted Resistor DAC and obtain expression for n-bits.
    ii. Sketch the Analog output voltage for the given digital input code. **(Sep 06, May 05)**
    iii. What are the major disadvantages in this type?

34. Give the working principle of Analog-Multiplexer. Give block diagram of a input analog multiplexer using CMOS gates and explain how it works. **(Sep 06, Nov 04)**

35. i. List out different types of A/D converters and compare their merits and demerits.
ii. Give the schematic circuit of an A/D converter widely used in digital voltmeters and explain its operation. Derive expression for output voltage. **(Sep 06, Dec 04)**

36. Draw the complete Block Schematic circuit including gating circuit, level amplifiers of R-2R 4 bit D/A converter and explain its operations. Derive expression for its output voltage V_0. **(May 06, 04)**

37. Compare weighted resistor D/A converter and R-2R D/A converter **(May 06, 04)**

38. i. Why successive approximation A/D converters faster than dual-slope A/D converter? Explain.
ii. Draw the complete schematic circuit of successive approximations A/D converter and explain operations of this system. **(May 06)**

39. i. With a neat circuit diagram explain the functioning of an inverted R-2R ladder type Digital to Analog converter.
ii. The LSB of a 10-bit DAC is 20 m volts.
a. What is its percentage resolution? **(May 06, 05)**
b. What is its full-scale range?
c. What is the output voltage for an input, 10110 01101?

40. i. Explain the operation of a counter type of Analog to Digital converter.
ii. Specify the modifications necessary in the circuit for a time varying analog input voltage.
iii. Calculate the conversion time for a full scale input incase of a 12-bit counter type Analog to Digital converter driven by 2MHz clock. **(May 05)**

41. Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage Vo.**(May 05)**

42. A monochrome video signal that ranges from 0 to 8V, is digitized using an 8-bit ADC.
i. Determine the resolution of the ADC in V/bit
ii. Calculate the mean squared quantization error
iii. Suppose the ADC is counter controlled. The counter is up count and positive edge triggered with clock frequency 1MHz. What is the time taken in second to get a digital equivalent of 1.59 V? **(GATE 01)**

43. Draw a neat schematic to show the functional blocks of a successive approximation A/D converter. Explain its operation using timing diagrams. Comment on its conversion speed with respect to the speeds of parallel A/D converter and dual slope A/D converter. **(IES 03)**

44. Compare the maximum conversion time of an 8-bit digital ramp ADC with that of a successive approximation ADC both using a clock of 100 kHz. How do these compare with that of a flash type ADC? **(IES 03)**

UNIT-VI

1. a) Sketch CMOS NAND gate and explain its working.
b) What is meant by Tri-static logic? Draw the circuit of Tri-state TTL logic and explain its functions. **(Nov 13)**

2. i. Why are tristated outputs and open collector output used in TTL ICs? List the advantages for both types of outputs.
   ii. List the differences between various logic family ICs under TTL family like 74 series, 74F series, 74 ALS series, 74 AS series ICs. **(Nov 12)**

3. i. Design a CMOS transistor circuit with the functional behavior

   ii. Distinguish between static and dynamic power dissipation of a CMOS circuit? Derive the expression for dynamic power dissipation? **(Dec 11)**

4. i. What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values of a CMOS NAND gate.
   ii. Design a CMOS 4-input AND-OR-INVERT gate. Draw the logic diagram and function table. **(Dec 11)**

5. i. Explain the effect of floating inputs on CMOS gate.
   ii. Explain how a CMOS device is destroyed.
   iii. What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic. **(Dec 11)**

6. i. Draw the circuits of NAND and NOR gates using CMOS logic and explain their operation with truth tables.
   ii. Compare the performance of various logic families with reference to power dissipation, propagation time delay, Fan in and Fan out. **(Dec 11)**

7. Specify the following parameters for 74H CMOS:
   i. $V_{OL(max)}$
   ii. $V_{OH(min)}$
   iii. $V_{IL(max)}$
   iv. $V_{IH(min)}$ **(May 11, 09. Nov 10)**

8. Specify the following parameters for 74 TTL :
   i. $I_{OL(max)}$
   ii. $I_{OH(min)}$
   iii. $I_{IL(max)}$
   iv. $I_{IH(min)}$ **(Nov 10)**

9. i. Sketch CMOS NAND Gate and explain its working
   ii. Sketch CMOS NOR Gate and explain its working. **(Nov 10)**

10. i. Explain the classification of integrated circuits.
    ii. Sketch TTL NAND Gate and explain its working
    iii. Sketch TTL NOR Gate and explain its working **(Nov 10)**

11. i. Draw the circuit of a Totem-pole TTL NAND gate ? What is the purpose of using a diode at the output stage ? Explain its operation and verify the truth table.
    ii. When do we use open-collector TTL gate?
    iii. Which is the fastest logic gate and why ? **(Nov 10, Aug 08, May 10, 04)**

12. Explain the classification of integrated circuits **(Nov10, May10, 09)**

13. i. Draw the schematic circuits of CMOS NAND and CMOS NOR gates and explain their functions with the help of Truth-Table.
    ii. What are the advantages and disadvantages of CMOS over TTL gate?
    iii. Which is the fastest saturated logic gate? and Why? **(Nov 10, Apr 08)**

14. i. Compare different logic families and mention their advantages and disadvantages?
    ii. Which is the fastest non-saturated logic gate? Draw the circuit and explain its functions.
    (May 10, 05,Aug 07)

15. i. Draw the circuit of two input NAND gate with totem-pole output and do the static analysis when output is HIGH & Output is low.
    ii. Explain why two totem pole outputs can't be tied together.
    iii. With neat circuit explain the concept of open collector O/P with pull-up. resistor. **(May 10)**

16. i. Explain sinking current and sourcing current of TTL output? Which of the above parameters decide the fan out and how?
    ii. Distinguish between static and dynamic power dissipation of a CMOS circuit? Derive the expression for dynamic power dissipation? **(May 10)**

17. i. With the help of a neat circuit diagram, explain the working of
    a. MOS inverter.
    b. Two input MOS NAND gate.
    ii. Find the logic output of a TTL NAND gate that has all its inputs unconnected. **(Jan 10)**

18. i. With the help of neat circuit diagram explain the working of a
    a. Two input CMOS NAND gate.
    b. CMOS inverter.
    ii. Explain TTL to CMOS and CMOS to TTL interfacing. **(Jan 10)**

19. i. Explain the following with reference to a gate
    a. Fan-in.
    b. Fan-out.
    c. Propagation delay.
    d. Noise margin.
    e. Speed power product.
    ii. What are the merits and demerits of TTL family? **(Jan 10)**

20. i. Compare TTL, ECL, IIL, MOS and CMOS logic families with respect to fan in, fan out, noise margin and propagation delay.
    ii. With the help of neat circuit diagram explain the working of Two input TTL NAND gate. **(Jan 10)**

21. i. Define logic family and explain
    ii. Sketch TTL OR Gate and explain its working
    iii. Sketch TTL AND Gate and explain its working. **(May 09)**

22. A 74LS TTL gate drives four 74HC CMOS gates. Minimum Vcc is 4.75 V. Determine the minimum value of pull-up resistor for interfacing these devices.(VOL(max)=0.4V, IOL=8mA and IIL=-1microA
    i. Explain TTL inverter with open collector output.
    ii. Compare various logic families
    iii. Differentiate bipolar IC and MOS IC. **(May 09)**

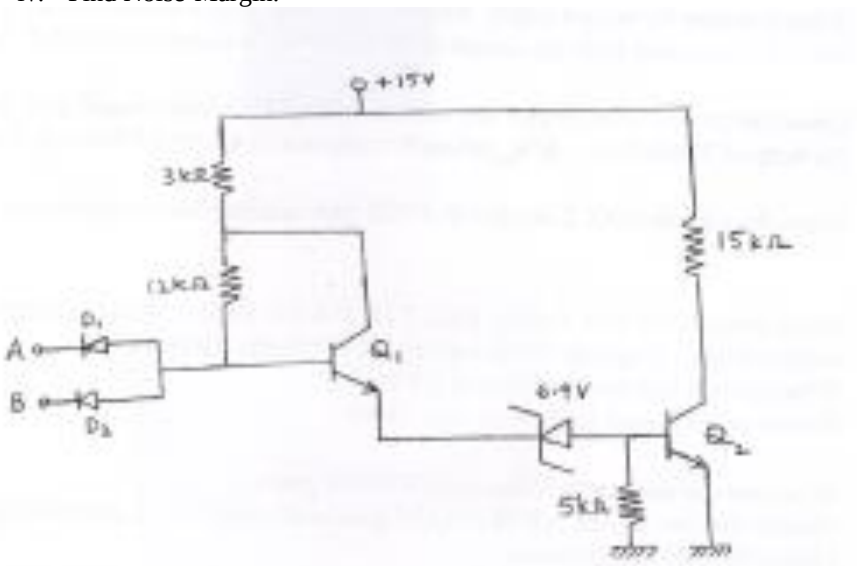
23. i. What is meant by Tri-state logic ? Draw the circuit of Tri-state TTL logic and explain its functions.
    ii. Draw the schematic circuit of TTL active pull-up NAND gate and explain its operation with the help of Truth-Table. **(Aug 08, 07)**

24. i. Realize the given expression y = AB + CD using N-MOS logic and verify it. What is the name of the given function and what is its advantage?
    ii. Compare the relative merits of NMOS, CMOS, TTL and ECL logic families. **(Aug 08, 06, May 05)**

25. For the given circuit shown below **(Aug, Apr 08, May 06)**
    i. Explain the operations of the circuit with the help of Truth-Table.
    ii. If h_{FE} of Q_1 is 30, find h_{FEmin} of Q_2

iii. If hFE of Q_2 is 30, what is Fan-Out?

iv. Find Noise-Margin.



26. List out advantages, disadvantages & applications of MOS logic. **(May 08)**

27. i. Explain the operation of open drain output of CMOS? **(May 08)**
    ii. Explain the behavioral difference between simple transistor logic inverter and Schottky logic inverter?

28. i. Explain the following terms with reference to TTL gate?
    a. Logic levels.
    b. DC Noise margin.
    c. Low-state unit load. iv. High-state fan out.
    ii. List out TTL families and compare them with reference to propagation delay, power consumption, speed-power product and low level input current? **(May 08, Aug 07)**

29. i. Define **(May 08, 05)**
    a. Positive logic b. Negative logic. c. Pulse logic.
    ii. What is meant by AOI logic. Explain with help of an example.

30. List out standard TTL Characteristics and explain them briefly with necessary diagrams. **(May 07)**

31. i. Design CMOS transistor circuit for 2-input AND gate? With the help of function table explain the circuit?
    ii. Draw the resistive model of a CMOS inverter and explain its behavior for LOW and HIGH outputs? **(May 07)**

32. i. Design a 4-input CMOS OR-AND-INVERT gate? Explain the circuit with the help of logic diagram and function table?
    ii. Explain the following terms with reference to CMOS logic?
    a. Logic Levels
    b. DC Noise margin
    c. Power supply rails
    d. Propagation delay **(May 07)**

33. i. Draw the logic diagram equivalent to the internal structure of an 8-input CMOS NAND gate? Show the transistor circuit for this gate and explain the operation with the help of function table?
    ii. Draw the circuit diagram of basic CMOS gate and explain the operation? **(May 07)**

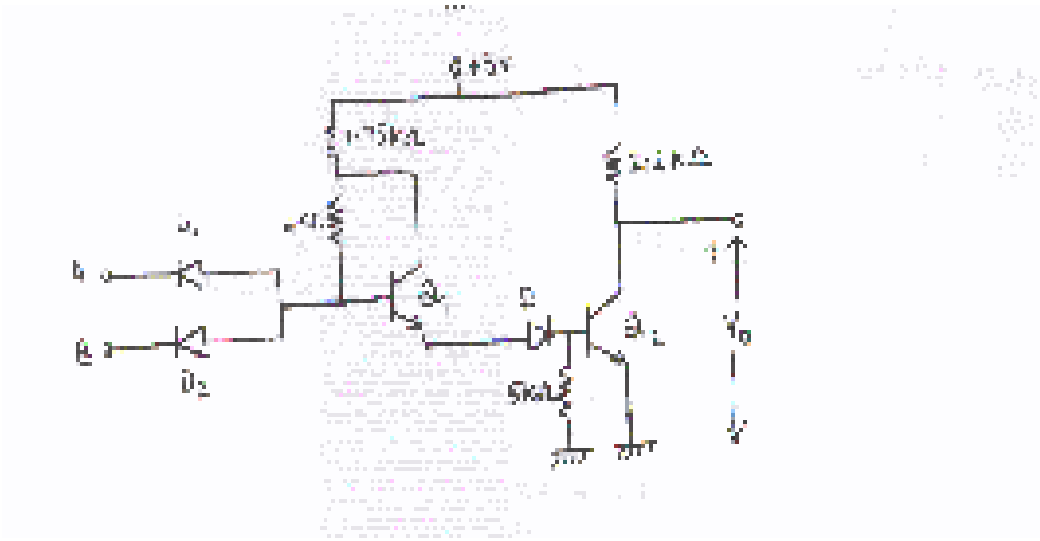
34. i. Define the terms (i) Positive Logic (ii) Negative Logic **(May 06, 05)**
    ii. Show that Positive logic EX-OR operation is equivalent to negative logic EX-NOR operation.

35. Draw the circuit 3 input D.T.L. NAND gate and explain its operation with the help of truth-table. How can you improve the Fan-out of the circuit. Explain with the help of modified circuit. **(May 06, 05)**

36. i. Compare different logic families and mention their advantages and disadvantages?
ii. Which is the fastest non-saturated logic gate? Draw the circuit and explain its functions. **(May 05)**

37. Draw the circuit of ECL logic OR/NOR gate and explain its functions. **(Sep 06, May 05,Dec 04)**

38. For the given circuit explain its operation with the help of Truth Table. Find h_{FEmin}, Fan-out if h_{FE}=30, and Noise-Margin for the given circuit shown below. (Assume all the active devices are made of silicon).



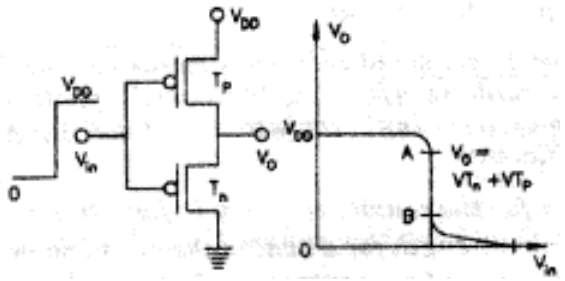
(May 05)

39. Explain the following with suitable circuit diagrams: **(Dec, May 04)**
i. Totem-pole TTL gate
ii. ECL gate
Are they called universal gates ? Justify your answer.

40. i. List out the advantages of CMOS logic.
ii. Draw the circuit of CMOS NOR gate and verify the Boolean function.
iii. Give the working principle of 12 L logic with neat circuit diagram. **(Dec 04)**

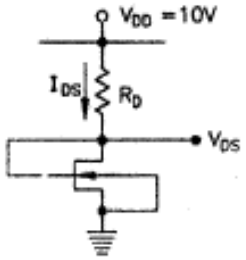
41. .i. When do we prefer H.T.L. (High-Threshold Logic) gate? And explain why?
ii. Draw the Integrated circuit of H.T.L. 3-input NAND gate, and explain its operation with the help of Truth Table.
iii. Find out the average power dissipation of the gate. **(Dec 04)**

42. A typical CMOS interval has the transfer characteristics (VTC) (V_0-V_{in}), as shown in the fig. Below. Evaluate the value of the Inverter threshold, V_{inx}, which is the value of the input at which V_o falls abruptly by $DV_0=V_{Tn} + T_p$.
Given $b_n = m_nC_{ox}$ (W/L)n = $b_p = m_pC_{ox}$ (W/L) p
V_{Tn}=1V, V_{Tp}=-1V and V_{DD}=5V

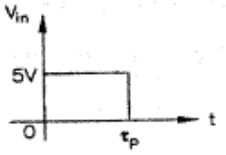


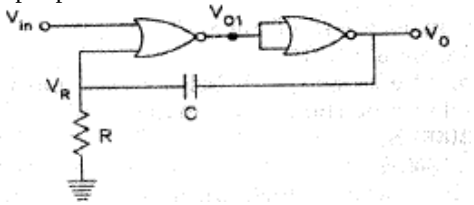
(GATE 94)

43. Given an NMOS circuit as shown in Fig. The specifications of the circuit are:
V_{DD}=10V; b = K=$m_n C_{ox}$(W/L) = 10^{-4} Amp/ V^2
V_T=1V and I_{DS} = 0.5 mA.
Evaluate V_{DS} and R_D for the circuit. Neglect body – effect for V_T. **(GATE 97)**



45. For the CMOS monostable multivibrator of Fig., R=50 kW, C=0.01 mF, V_{DD}=5V, and the CMOS NOR gates have a threshold voltage (V_T) of 1.5 V. v_{in} is a trigger pulse (t_p<<RC) as shown in the figure.
   i. Plot v_{01} and v_R as function of time.
   ii. Write the equation for v_R(t), for t>0.
   iii. Find the time period of the output pulse **(GATE 00)**





47. i. Draw the circuit diagram of a two input TTL NAND gate and label component and write function table.
   ii. Draw a typical input-output transfer characteristic of a TTL inverting gate. **(IES 98)**
   iii. Define fan out. Which factor is responsible for the limit of fan out in TTL circuits
   iv. "Loading an output with more than its rated fan out has several effects". Write at least five effects

UNIT-VII

1. a) Explain how to use multiplexer as a logic function generator
   b) Explain 4-bit parallel binary subtractor circuit using 2's Complement system. **(Nov 13)**

2. i. Draw the pin diagram of 74 series decoder IC and explain its functioning. Explain how Boolean functions can be generated using decoders through an example.
   ii. List out the 74 series IC No s for code converters to translate BCD-to-seven-segment display and BCD-to-gray scale. Draw pin diagrams. **(Nov 12)**

3. i. With the help of logic diagram explain 74157 multiplexer.

ii. Design a full subtractor with logic gates?
iii. Using the above subtractor design a 8-bit ripple subtractor. **(Dec 11)**

4 i. Using two 74x138 decoders design a 4 to 16 decoder?
ii. Realize the following expression using 74x151 IC?
(Dec 11, May 10)

5. i. Give the logic diagram of 74x139? Explain with the help of truth table? Using this device design a 3 to 8 decoder and provide the truth table?
ii. Design a 16-bit comparator using 74x85 ICs? **(Dec 11)**

6. i. Draw the CMOS circuit diagram of tri-state buffer. Explain the circuit with the help of logic diagram and function table.
ii. Design a CMOS transistor circuit that realizes the following Boolean function.
Also explain its functional operations. **(Dec 11)**

7 Explain the 74154 4-line to 16 line decoder with logic diagram and logic symbol. **(May 11)**

8. Explain and design the leading zero suppression using BCD / 7 -Segment display **(Nov 10)**

9. Design 4:1 Mux with logic diagram and symbolic representation. **(Nov 10)**

10. Convert the binary numbers to gray codes using Ex- OR gates
i. 1001
ii. 11001111
iii. 10000001
iv. 10011 **(Nov 10)**

11. i. Draw the logic diagram of 74x283 IC and explain the operation?
ii. Write short notes on BCD to binary converter? **(May 10)**

12. i. Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram.
ii. Write short notes on full subtractor. **(May 10, 07)**

13. i. Give the logic diagram of 74x147 and explain its truth table?
ii. Write short notes on half subtractor? **(May 10)**

14. i. Design a 4-bit binary to gray code converter and draw the circuit.
ii. Design 4 multiplexer using gates. What are the applications of a multiplexer? **(Jan 10)**

15. Briefly explain the operation of the following
a. Encoder.
b. De multiplexer.
c. Decoder.
d Multiplexer. **(Jan 10)**

16. i. Design a four bit adder/ subtractor circuit with Add/subtract control lines.
ii. Design Full adder using 41×multiplexer.
iii. Design 1-bit Comparator circuit and draw the circuit diagram. **(Jan 10)**

17. i. Design a 3-bit odd parity generator and checker circuits.
ii. Draw the circuit and explain the operation of parallel binary adder/subtractor circuit using 2'scomplement.

18. Design 8 - bit adder using 7482. **(May 09)**

19. Design and explain the following

i. Basic comparator operation
ii. Logic diagram for comparison of 2- bit binary numbers. **(May 09)**

20. Explain application of an encoder using a keyboard encoder. **(May 09)**

21. i. What are the basic blocks of analog multiplexer? Explain how the data selection process in performed in it.
ii. Draw a sample and hold circuit and explain its operation with necessary input and output waveforms and indicate its uses. **(Aug 08)**

22. i. Write short notes on n- Bit parallel adder. **(May 08)**
ii. Design a driver circuit for LCD display.

23. i. What is multiplexer? Draw the logic diagram of 4 to 1 line multiplexer?
ii. Design half adder using NAND gates only? **(May 08, Aug 07)**
24. i. Design 1:8 Demultiplexer using two 1:4 Demultiplexer?
ii. Realize the following expression using 74x 151 ICs and74x 139 IC
$F(Z) = ABCD + ABCD + ABCD + ABDE + ACDE + ABCE + ABCD$ **(May 08, May 07)**

25. i. Design a serial binary adder?
ii. Design a full subtractor with logic gates? **(Aug 07)**
26. i. What is the necessity of tri state buffer?
ii. Design a 16-bit comparator using 74×85 ICs? **(Aug 07)**
27. i. Draw the circuit for 3 to 8 decoder and explain?
ii. Write short notes on half adder? **(May 07)**
28. Describe encoding and give an example **(R4-Ch6)**

30. Discuss the basic structure of parallel binary adder. Show how two 74LS83A can be connected to form an 8-bit parallel adder. (**R4-Ch6)**

31. Discuss the basic structure of parallel binary adder. Use 74LS283 adders to implement a 12 bit-parallel adder. **(R4-Ch6)**

32. What does a comparator do. Use 74HC85 comparators to compare the magnitudes of two 8-bit numbers. Show the comparators with proper connections. **(R4-Ch6)**

33. What is the basic function of decoder. Determine the logic required to decode the binary number 1011 by producing a HIGH level on the output. **(R4-Ch6)**

34.. i. Convert the binary number 0101 to Gray code with exclusive OR gates.
ii. Convert the Gray code 1011 to binary with exclusive –OR gates. **(R4-Ch6)**

35. i. Convert the BCD number 10000101 to binary
ii. Draw the logic diagram for converting an 8-bit binary number to gray code. **(R4-Ch6)**

36. What is the basic function of Multiplexer. Use 74LS151s and any other logic necessary to multiplex 16 data lines onto a single data output line. **(R4-Ch6)**

37. Briefly describe the purpose of each of the following devices
i. 74LS157 ii. 74LS48 iii. 74LS139 **(R4-Ch6)**

38. Implement the logic function specified in table given below using a 74LS151 8-input data selector/multiplexer. Compare this method with a discrete logic gate implementation. **(R4-Ch6)**

UNIT-VIII

1. a) Using the method of flip-flop conversion carry out the following conversions.
   i) S-R to T
   ii) J-K to D
   b) Describe the operation of an asynchronous decade counter **.(Nov 12)**

2. Design a 3-bit synchronous counter using JK flip-flops **.(Nov 12)**

3. i. Design a 3-bit LFSR counter using 74x194? List out the sequence assuming that the initial state is 10.
   ii. Design a Modulo-12 ripple counter using 74x74. **(Dec 11)**

4. i. Design a 4-bit binary synchronous counter using 74x74.
   ii. Design a modulo-60 counter using 74x163 ICs. **(Dec 11)**

5. i. Draw the D flip flop and T flip flop and explain the operation with truth table.
   ii. Draw the J-K flip-flop and explain its operation with truth table. **(Dec 11)**

6. i. Design a conversion circuit to convert a T flip-flop to J-K flip-flop?
   ii. Write short notes on:
   i. Edge triggered flip-flop
   ii. Master slave flip -flop. (**Dec 11)**

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulse 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z=1 and overlapping being allowed.
   i. Obtain State - Diagram
   ii. Also obtain state - Table
   iii. Find equivalence classes using partition method & design the circuit using D flip-flops. **(May 11)**

8. i. Explain with neat sketch how four bits 1110 are serially entered into the shift register.
   ii. Explain with neat sketch how four bits 1110 are serially shifted out of the shift register. **(Nov 10)**
9. i. Draw five stage synchronous binary counter using D flip flop
   ii. Draw complete timing diagram for the same. **(Nov 10)**

10. Write short notes on Clocked D flip flop **(May 10)**

11. Design MOD 5 synchronous counter. **(May 10, 08)**

12. Draw the logic diagram of binary counter and explain its operation? **(May 10)**

13. i. Design a conversion circuit to convert a D flip-flop to J-K flip-flop?
   ii. Design a 4-bit binary synchronous counter using 74×74? **(May 10, 07)**

14. Explain with an example why asynchronous input are required in flip-flops. **(May 10, 08)**

15. Design MOD 6 synchronous counter. **(May 10, 08, Aug 07)**

16. i. Explain the operation of J K, D and T flip flops with the help of a circuit diagram using NAND gates and truth table.
    ii. Design a 4-bit synchronous up counter using T-flip-flops. **(Jan 10)**

17. What is a decade counter? Design a 4-bit synchronous decade counter. Write the output sequence **(Jan 10)**

18. i. Distinguish between Synchronous and Asynchronous Counters.
    ii. Explain various configurations of shift registers. What are its applications? **(Jan 10)**

19. i. Explain the operation of S-R and J-K flip-flops with the help of circuit diagram and truth table. Also derive excitation tables.
    ii. What are the demerits of J-K flip flop. How do you overcome it? **(Jan 10)**

20. Explain 74194 four bit bidirectional universal shift register with block diagram and timing diagram. **(May 09)**

21. i. Find a modulo-6 gray code using k-Map & design the corresponding counter.
    ii. Compare synchronous & Asynchronous. **(May 09)**

22. i. Distinguish between Combinational circuits and sequential circuits. **(May 08)**
    ii. Write short notes on Clocked SR flip flop.

23. i. Distinguish between combinational and sequential circuit.
    ii. Define the following terms as applied to flip flops.
    a. Set up time b. Hold time c. Propagation delay
    d. Maximum clock frequency e. Power dissipation **(Aug 07)**

24. i. Explain 4 bit serial in parallel out register.
    ii. Draw the circuit of edge trigged SR flip flop made up of by basic gates & explain the operation. Sketch the wave form. **(Aug 07)**

25. Write short notes on synchronous up counter. **(Aug 07)**

26. i. Discuss in detail ROM access mechanism with the help of timing waveforms?
    ii. Write short notes-on Clocked Tflip-flop. **(May 07)**

27. i. Write short notes on serial in parallel out shift register.
    ii. Design a conversion circuit to convert a D flip-flop to T flip-flop? **(May 07)**

28. Explain with logic diagram and timing relationship of a master-slave flip-flop and edge triggered flip-flop**.** **(R4-Ch7)**

29. Define edge triggered flip-flops **(R4-Ch7)**

IC APPLICATIONS

Assignment Questions

UNIT-1

1. What is a level translator circuit? Why it is used with the cascaded differential amplifier?
2. List and compare ideal and practical characteristics of an Op-Amp.
3. An op-amp has a slew rate of 2V/μs. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation. Derive the formulae used.
4. What are the three differential amplifier configurations? Compare and contrast these configurations.
5. Draw the circuit diagram and explain the operation of an inverting amplifier, obtain the expression for closed loop voltage gain.

UNIT-2

1. Draw a circuit using Op-Amp, which can work as adder (inverting and non-inverting) and explain how it works.
2. Explain Practical integrator with suitable mathematical expression
3. Explain the operation and derive the expression for the overall gain of the op-amp instrumentation amplifier
4. Draw the circuit and explain the working of

1. voltage to current converter
2. current to voltage converter

3. Design a differentiator using Op-amp to differentiate an input signal that varies in frequency from 1KHz to 10KHz
4. Draw any one multivibrator circuit using Op-amp and explain its operation and derive relevant expression for its time period

UNIT-3

1. Design a second order low pass filter at a high cut off frequency of 1 KHz. Derive the transfer function of the filter.
2. Derive the expression for frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit
3. What is an all pass filter? Explain its operation and applications areas.
4. With a neat diagram explain about triangular wave generator
5. Design a wide band pass filter with f_L = 200Hz , f_H = 1 KHz and a pass band gain = 4.
   i. Draw the frequency response plot of this filter.
   ii. Calculate the value of Q for the filter.

UNIT-4

1. Explain the operation of 555 timer based Monostable multivibrator with functional diagram?
2. Draw and explain the functional block diagram of IC 555.
3. Explain the operation of Astable multivibrator using 555 timer.

4. Give the block diagram of NE 565 PLL and explain the role of each block. Make circuit connections to track the incoming signal and explain its operations
5. Draw the circuit of Schmitt trigger using 555 timer and explain its operation.

UNIT-5

1. Explain the operation of a dual slope type Analog to Digital converter.
2. Write short note on:
   i.R-2R Ladder DAC
   ii. Inverted to R-2R Ladder
3. Explain Functional diagram of successive approximation ADC
4. The LSB of a 10-bit DAC is 20 m volts.
   a. What is its percentage resolution?
   b. What is its full-scale range?
   c. What is the output voltage for an input, 10110 01101?

5. Explain the operation of parallel comparator type ADC with the help of a neat diagram

UNIT-6

1. Draw the circuits of NAND and NOR gates using CMOS logic and explain their operation with truth tables.
2. Compare the performance of various logic families with reference to power dissipation, propagation time delay, Fan in and Fan out.
3. Why are tristated outputs and open collector output used in TTL ICs? List the advantages for both types of outputs.
4. Draw the circuit of a Totem-pole TTL NAND gate ? What is the purpose of using a diode at the output stage ?Explain its operation and verify the truth table
5. Explain the following with reference to a gate
   a. Fan-in.
   b. Fan-out.
   c. Propagation delay.
   d. Noise margin.
   e. Speed power product

UNIT-7

1. Briefly explain the operation of the following
   a. Encoder.
   b. De multiplexer.
   c. Decoder.
   d Multiplexer.

2. Draw the circuit and explain the operation of parallel binary adder/subtractor circuit using 2'scomplement.

3. Realize the followingexpression using 74x 151 ICs and74x 139 IC
   $F(Z) = ABCD + ABCD + ABCD + ABDE + ACDE + ABCE + ABCD$
4. Design a 4-bit binary to gray code converter and draw the circuit.
5.Explain and design the leading zero suppression using BCD / 7 -Segment display

UNIT-8

1. Using the method of flip-flop conversion carry out the following conversions.
   i) S-R to T
   ii) J-K to D

2. Explain 74194 four bit bidirectional universal shift register with block diagram and timing diagram

3. Define the following terms as applied to flip flops.
   a. Set up time b. Hold time c. Propagation delay
   d. Maximum clock frequency e. Power dissipation
4. Design a 4-bit synchronous up counter using T-flip-flops

5.What is a decade counter? Design a 4-bit synchronous decade counter. Write the output sequence